Programmable Digital Delay Generator

Model 7030A

INSTRUCTION MANUAL

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INSTRUCTION MANUAL

We've moved:
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Warranty

Berkeley Nucleonics Corporation warrants all instruments, including component parts, to be free from defects in material and workmanship, under normal use and service for a period of one year. If repairs are required during the warranty period, contact the factory for component replacement or shipping instructions. Include serial number of the instrument. This warranty is void if the unit is repaired or altered by others than those authorized by the Berkeley Nucleonics Corporation.

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Parts List: 31

Input/Output Board 7030A-4 (649-059)
DL1 ECLDM-35 (Logic Delay) (316-019)
Output Amplifier 7030A-5 (649-057)
Logic Board 7030A-2 (649-064)

- CONTENTS -

Parts List (continued):

Oscillator Board	(649-050)
Thumbwheel Switch Board	(649-063)
Oscillator Interface 7030A-6	(649-083)
Panel Controls and Connectors	

Schematic Diagrams:	Dwg. No.
Oscillator	7030A-30
Logic Timing Circuits, ECL	7030A-31
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DIGITAL DELAY GENERATOR
MODEL 7030A

The Model 7030A is a NIM compatible instrument that provides digitally selectable time delays from 0 to 99.999 us. Delays are selectable in 1 ns increments. A gate output equal to delay times over 10 ns is also provided.

The Model 7030A's Initial and Delayed Pulse outputs are fixed in amplitude and continuously variable in width. External triggering is adjustable with a ± 2 volt threshold range selector for both positive and negative-going slopes. A $\pm 1/2$ clock period indeterminacy between the trigger and output pulses is automatically eliminated by trigger synchronizing circuitry that reduces indeterminacy to zero.

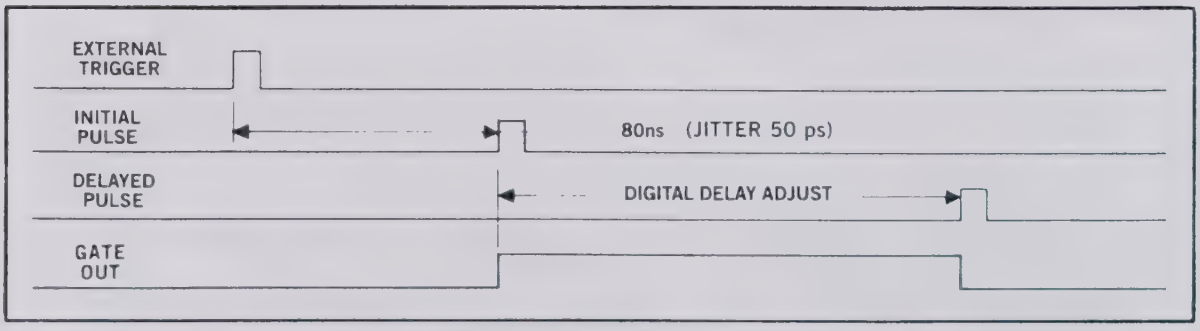
SECTION 1

SPECIFICATIONS

DELAY & GATE SELECTION	0 to 99.999 us in 1 ns increments.
ACCURACY	
Delay:	1 to 9 ns, ±0.1 ns; 10 to 99 ns ±0.3 ns; 100 ns-full range, ±0.5 ns ± time setting X time base error.
Gate:	Delay interval ±2 ns (fixed).
TIME BASE STABILITY	1 x 10^{-5}/°C
INSERTION DELAY	Ext. Trigger to Initial Pulse, 80 ns.
INDETERMINACY	None.
JITTER	
External Trigger to Initial Pulse	50 ps rms max.
Between Initial and Delayed Pulses	1 to 999 ns, 100 ps rms max; 1 to 99 us, 150 ps rms max.
TRIGGER MODES	
External:	Rate 0 to 10 MHz; 10 ns minimum width; 250 mV minimum amplitude; 50 ohm nominal input impedance. Trigger level control ±2 V continuously adjustable. Positive or negative slope selection switch.
Single Cycle:	Panel pushbutton.
OUTPUT PULSES	
Initial and Delayed	Positive, +5 V into 50 Ohms; 3 ns rise and fall time; width continuously adjustable, 15 ns to 1 us. Negative, -2 V from 50 Ohms; 3 ns rise and fall times; width continuously adjustable, 15 ns to 1 us.
Gate	+ 5 V into 50 Ohms; 3 ns rise and fall times.
DIMENSIONS	4.05" W x 8.70" H x 10.50" D 103x221x267 mm).

- SPECIFICATIONS -

WEIGHT	4.5 pounds net (2 kg); 8 pounds shipping (3.6 kg).
AMBIENT	0°C to 50°C (32° F to 122° F)
POWER	+6 V, 550 mA; -6 V, 1.3 A; +12 V, 430 mA; -12 V, 380 mA; -24 V, 200 Ma.
REMOTE PROGRAMMING	Data Input: BCD coding, TTL compatible; V(High) = 0; V(Low) = 1 Data Strobe: TTL compatible; V(Low) = Strobe. Remote/Local: TTL compatible; V(High) = Local; V(Low) = Remote. Reset: TTL compatible; V(low) = Reset. Programming Time: 0.5 us maximum. Chassis Connector: Amphenol 57-40360.
AUXILIARY MODULES	Instrument modules are available to boost Initial and Delayed Pulse amplitudes to higher voltages and interface the 7030A for IEEE-488 GPIB programming.



Relationship between waveforms

SECTION 2

OPERATING INFORMATION

2.1 GENERAL

This section will familiarize the operator with the functional capabilities of the Model 7030A Digital Delay Generator. Operating controls, connectors and operating procedures are covered.

2.1.1 PERFORMANCE INFORMATION

The circuitry of the Model 7030A synchronizes the internal clock with external triggers to provide outputs devoid of clock-phase uncertainty, thus generating outputs with low jitter and no indeterminacy with respect to the input trigger.

Time reference levels between the Model 7030A outputs should be at the 50% amplitude point of each pulse. Rise and fall time specifications are between the 10% and 90% points of the outputs. Care must be taken to match external cables if the accuracy of the unit is to be maintained (Para. 2.1.3).

---NOTE---
The switch on the rear panel of the 7030A must be in the OPERATE position in order to use the instrument.

2.1.2 OPERATING TEMPERATURE

The internal frequency reference of the unit is enclosed in an oven for stability. The unit should be allowed to warm up for 45 minutes before high-precision timing is done.

2.1.3 CABLES, ATTENUATORS AND OSCILLOSCOPES

The various outputs of the Model 7030A contain frequency components in excess of 100 MHz. All signal handling components such as loads, attenuators, cables, connectors and oscilloscopes should be able to handle these signals without distortion in order to maintain the inherent accuracy of the unit.

---NOTE---
Some sampling oscilloscopes have maximum input ratings that may be exceeded by the outputs of the Model 7030A. In such cases use a signal attenuator.

As all tests made with the unit should be made as close as possible the output connectors and at the 50% points of the outputs The effect of cables in both distorting and delaying the signals is important. Such phenomenon should always be considered when making critical measurements. For example, one foot of RG58/U cable has a delay of 1.5 ns. Therefore, if cables from the INITIAL and DELAYED outputs are different in length by only 1.5 inches, the delay error induced will be greater than ±100 ps - the inherent accuracy of the unit. Also, should an impedance mismatch occur in one of the cables, it is possible that reflections could occur at the 50% point of the waveshape adding further to the error.

2.2 OPERATING CONTROLS AND CONNECTORS

2.2.1 DC POWER VOLTAGES

The DC power requirements for the Model 7030A are noted in the specifications. Normally, the Model 7030A is in a NIM-type power supply that supplies all the necessary voltages. (Note that some NIM supplies do not offer the required full complement of six DC voltages.) Alternatively, other well regulated DC power sources, such as commercially available "OEM" and "slot" supplies, can be used to power the Model 7030A via an appropriate mating power connection available from Berkeley Nucleonics or other sources.

2.2.2 EXTERNAL TRIGGER INPUT CONNECTOR

A signal of the proper levels at this connector will trigger the unit. The input impedance is 50 ohms. For proper triggering these signals must have at least 250 mV peak-to-peak amplitude, 10 ns width and be 10 MHz or less in frequency. Peak inputs should not exceed 15 volts and the average power should not exceed 1/2 watt.

2.2.3 EXTERNAL TRIGGER SLOPE SWITCH

The SLOPE switch determines whether the instrument will trigger on a positive-going or negative-going transition at the EXT TRIG INPUT connector. The trigger level is determined by the EXT TRIG LEVEL control.

2.2.4 EXTERNAL TRIGGER LEVEL CONTROL

The EXT TRIG LEVEL control determines the voltage level at which the Model 7030A will trigger. The LEVEL control varies the threshold from approximately +2 volts fully clockwise to -2 volts

fully counterclockwise. Triggering occurs when the input signal passes through threshold by at least 100 mV and retriggering can occur after the input signal has dropped at least 100 mV below threshold.

2.2.5 SINGLE CYCLE TRIGGER PUSHBUTTON

The SINGLE CYCLE pushbutton generates one delay/gate cycle each time it is depressed.

2.2.6 MANUAL RESET PUSHBUTTON

The manual RESET pushbutton initiates a reset and maintains this condition as long as the button is depressed. Reset halts a delay/gate cycle that may be in progress and loads the data available at the output of the internal memory. Automatic reset normally occurs at the end of each delay/gate cycle. If the DELAY thumbwheel switches are changed between cycles, the old data is still loaded in the registers and will not be updated until the normal reset at the end of the next delay cycle. Pressing the manual RESET will update the new data into the instrument.

2.2.7 DELAY THUMBWHEEL SWITCHES

These switches set the time delay between the Initial and Delayed pulses and set the Gate time. Delays from 0 to 99.999 us are selectable. When a DELAY switch is changed during a delay cycle, the next delay/gate cycle will generate new delay and gate outputs. However, should the change occur between output intervals, the next delay/gate cycle after the change will cause a delay and gate with the old setting. All subsequent outputs will have the new setting. If the new delay setting is desired on the next cycle, pressing the RESET button will load in the new setting.

If remote programming is in use, the new delay can be implemented immediately by bringing the reset line low regardless of the timing (Para. 2.2.14).

2.2.8 INITIAL PULSE POSITIVE CONNECTOR

The POS INITIAL PULSE marks the beginning of a delay/gate cycle. The pulse is +5 volts in amplitude with a 50 ohm load. The amplitude is fixed while the width is variable from 15 ns to 1 us with front panel control (Para. 2.2.11).

Note that the best waveshapes are obtained when this output is terminated in 50 ohms. If a higher terminating impedance is to be used, better results will be obtained if a shunt impedance is used in parallel to simulate 50 ohm load.

2.2.9 INITIAL PULSE NEGATIVE CONNECTOR

The NEG INITIAL PULSE is time coincident with the POS INITIAL PULSE. Its amplitude is fixed at -2 volts from a 50 ohm source. When a 50 ohm load is used the amplitude is -1 volt. The width of this pulse is the same as the Initial Positive Pulse (Para. 2.2.11).

2.2.10 DELAYED PULSE POSITIVE AND NEGATIVE CONNECTORS

The Delayed pulses mark the end of the delay and gate period set by the DELAY thumbwheel switches or remote programming. These have the same characteristics as their initial pulse counterparts (Para. 2.2.8 and 2.2.9).

2.2.11 WIDTH CONTROLS

The WIDTH controls vary the output width of the pulses. The INITIAL PULSE POS and NEG widths are varied simultaneously by the left-hand WIDTH control while the DELAYED PULSE POS and NEG widths are varied simultaneously by the right-hand WIDTH control. Settings are variable from 15 ns to 1 us.

2.2.12 GATE OUTPUT CONNECTOR

The GATE OUT is a positive 5 volt pulse that has a leading edge occurring in coincidence with the leading edge of the Initial pulses and a trailing edge coincident with the leading edges of the Delayed pulses. This results in a pulse with a duration equal to the delay interval that is accurate to within $\pm$2 ns (fixed).

2.2.13 REMOTE OPERATION LIGHT

The REMOTE indicator lights to show when the Model 7030A is being controlled by a remote source. Details for remote programable operation are set forth below.

2.2.14 CALIBRATE-OPERATE SWITCH (Rear Panel)

A slide switch on the rear panel selects between normal operation and an oscillator calibration operation. Before installing the

instrument into a NIM power supply for normal use, be sure that the switch is in the OPERATE position. Otherwise the instrument will not provide outputs to the front panel.

2.2.15 PROGRAMMING CONNECTOR (Rear Panel)

This connector is the input for all data and control signals necessary to remotely program the Model 7030A. Each input has the characteristics of one standard TTL gate.

(1) REMOTE DATA INPUTS

The Remote Data Inputs determine the delay and gate intervals when the unit is being remotely programmed. Data are entered in parallel BCD format with V(high) = logical 0 and V(low) = logical 1. Table 2-1 provides the programming pin number assignments.

(2) STROBE

A Strobe pulse is used to transfer the data from the data lines to the internal memory. When the strobe line is at V(high) the unit will ignore signals on the data lines. When the strobe goes low, the internal memory accepts the data line information at that time. The Model 7030A will not recognize the new data in the latches until the end of a delay/gate cycle. If the unit is strobed during a delay/gate cycle, the next output will reflect the new data. If the unit is strobed after a delay/gate cycle, the next output will be the old data, and the second delay/gate after the strobe will reflect the new data. If the data must be transferred between cycles and an immediate update is necessary, it can be accomplished by bringing the reset line low after the strobe has occurred (Para. (3)).

----------NOTE----------
Minimum strobe width is 100 ns and data must be present and correct for 25 ns before and after the end of the strobe pulse. Pin assignment for the data strobe signal is given in Table 2-1.
---

(3) RESET

The Reset signal causes any delay/gate cycle in progress to terminate and data to be transferred from the memory to the internal counters for immediate use. If the unit receives both a strobe and a reset, the next output will

reflect the latest data. V(low) is the level for reset. See Table 2-1 for the pin assignment. Minimum reset pulse width is 100 ns.

(4) LOCAL/REMOTE CONTROL

A low level on this line causes the Model 7030A to operate in the remote mode with control being provided by a remote source. When this line is high or left open, operation is from the front panel DELAY switches. In this local mode, the remote strobe signal has no effect: V(low) = Remote and V(high) = Local. See Table 2-1 for pin assignment. When the Model 7030A is under remote programming control, the REMOTE indicator will be lit.

TABLE 2-1

Data	Pin #	Data or Control	Pin #
1 ns	1	10 us	9
2 ns	2	20 us	10
4 ns	19	40 us	27
8 ns	20	80 us	28
10 ns	3	Reset	17
20 ns	4	Data Strobe	18
40 ns	21	Local/Remote	35
80 ns	22	Ground	36
100 ns	5		
200 ns	6		
400 ns	23		
800 ns	24		
1 us	7		
2 us	8		
4 us	25		
8 us	26		

Remote programming connector (J901) is an Amphenol 57-40360 and requires a mating connector Amphenol 57-30360.

2.3 OPERATING INSTRUCTIONS

2.3.1 GENERAL

Some of the more common operating considerations and configurations are covered.

---NOTE---
The 7030A will not operate unless the slide switch on the rear panel is in the OPERATE position.

2.3.2 TURN-ON

For the most precise measurements, the Model 7030A should be allowed to warm up for 45 minutes so that the ovenized crystal oscillator has had time to stabilize.

2.3.3 TIME DELAY AND GATE WIDTH GENERATION

A thorough operational check of the unit's operation requires an external trigger source and an oscilloscope or other indicating device such as a TIM (Time Interval Meter). To generate outputs non-manually an external signal is connected to the EXT TRIG INPUT connector and the SLOPE and LEVEL controls are adjusted as required.

Set the desired delay/gate time with the thumbwheel switches. The Initial and Delayed pulse widths can be set with their individual front panel controls. The gate output is fixed in amplitude and has a width equal to the time between the leading edges of initial and delayed pulses.

2.3.4 MULTIPLE DELAYS AND WIDTHS

Because a Model 7030A exhibits very low jitter when triggered, it is possible to generate multiple, sequential and parallel delays and widths in any combination with very low jitter between pulse edges.

For parallel operation, trigger all Model 7030A's from the same source. If identical cables are used, the outputs from all units will be very close for the same settings. Fine adjustments can be made using the External Trigger Level control to vary the point on the input pulse at which each Model 7030A triggers.

For serial operation, the first unit can be triggered from an external source or manually. The next unit is then triggered from a delayed output of the first. If the Gate Output of the second unit is used, the waveshape obtained can be precisely set in both delay and width, with very low jitter between the trigger and any of the output pulse edges.

SECTION 3

CIRCUIT DESCRIPTION

3.1 GENERAL

The purposes of this section are:

1. Familiarize a user or maintenance technician, working with the Model 7030A, with the purpose and function of the instrument's principal circuits.

2. Provide enough design details for each of the principal circuits so that a technician will understand:

   a. Interaction between major segments comprising various circuits.

   b. Operating characteristics and interfacing of the circuits.

   c. Routing and logic relationships of the input and output signals.

   d. Limitations of the operating modes.

3. Provide the relevant block and timing diagrams.

4. Supply sufficient circuit function and design detail to maintain, troubleshoot and repair an instrument. Test and calibration procedures are separately described in Sect. 5.

Figs. 3-1 and 3-2 illustrate in block diagram form the relationship between the principal circuits of the Model 7030A. Fig. 3-1 includes all of the major instrument sections from input trigger to the output signals. The second figure, 3-2, is a detailed block diagram of the timing circuits. The reader should become familiar with these diagrams, as well as the waveshape diagrams and schematics, and refer to them frequently in order to better understand the circuit relationships explained in the text. A clear overview of the signal routings and relationships is also important.

Figs. 3-3 and 3-4 illustrate pulse timing at various test points (TP) on the identified circuit boards. The relationships shown are derived from a 123 ns digital time setting.

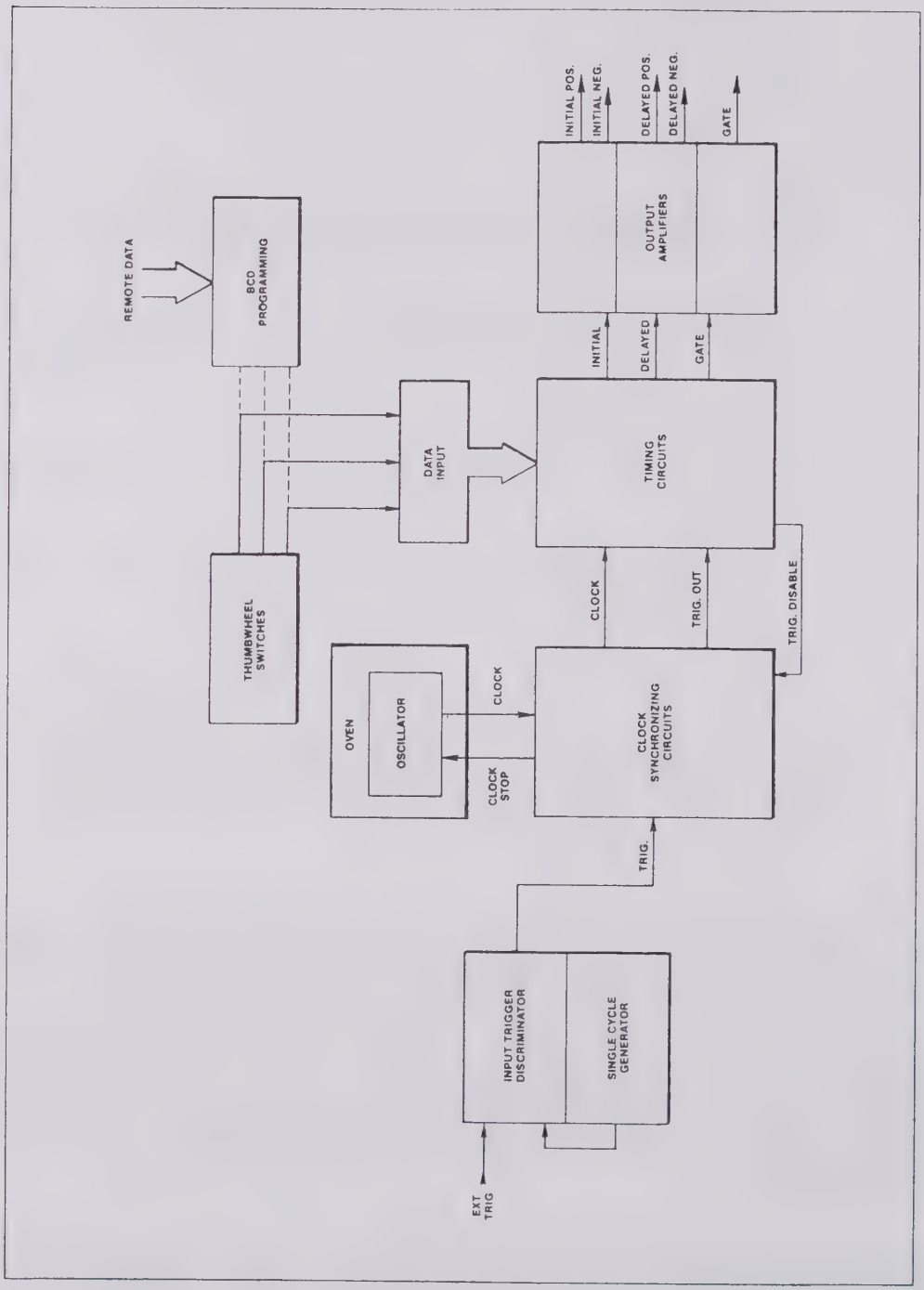


FIG. 3-1 Block Diagram showing the relationship between the major instrument sections from the power supplies through the timing circuits to the output signals.

3.2 CIRCUIT OPERATION AND FUNCTION

3.2.1 INTRODUCTION AND OVERVIEW (Fig.3-1, 3-2, 3-3, 3-4)

The Input circuit generates a clock stop signal which is initiated in one of the two following ways: 1) by an external trigger introduced to the instrument through the trigger discriminator, or 2) through a single cycle generator.

The clock stop signal is sent to Clock Synchronizing circuits to control the oscillator which, in turn, provides a clock signal phased with the trigger signal. The clock and trigger are then sent to the Timing circuits.

These Timing circuits produce an initial pulse and start a countdown process through the delay circuitry to generate a delayed pulse and a separate gate pulse whose leading edge coincides with the leading edge of the initial output pulse while its trailing edge coincides with the leading edge of the delayed output. These relationships are shown in Fig. 3-4.

Settings made with the Thumbwheel switches or remote data inputs select the desired number of nanosecond increments between the initial and delayed pulses. This data is processed by the Timing circuits to produce the initial, delayed and gate pulse differential drive signals which are then introduced to Output Amplifiers. The amplifiers condition these differential signals to provide TTL and "quasi" ECL outputs.

3.2.2. INPUT CIRCUITS (Fig. 3-1)

The two principal circuits that comprise the Input circuits. These are the Input Trigger Discriminator and Single Cycle Generator. Model 7030A is triggered externally or manually. It has no internal triggering capability.

A. Input Trigger Discriminator

This circuit is a comparator which converts the External Trigger Input signal to an ECL signal compatible with the instrument's internal control circuitry.

B. Single Cycle Trigger Generator

This circuitry is used to generate trigger signals during single-cycle operation. Its output signal is also converted to ECL form prior to entry into the Clock Synchronizing circuits.

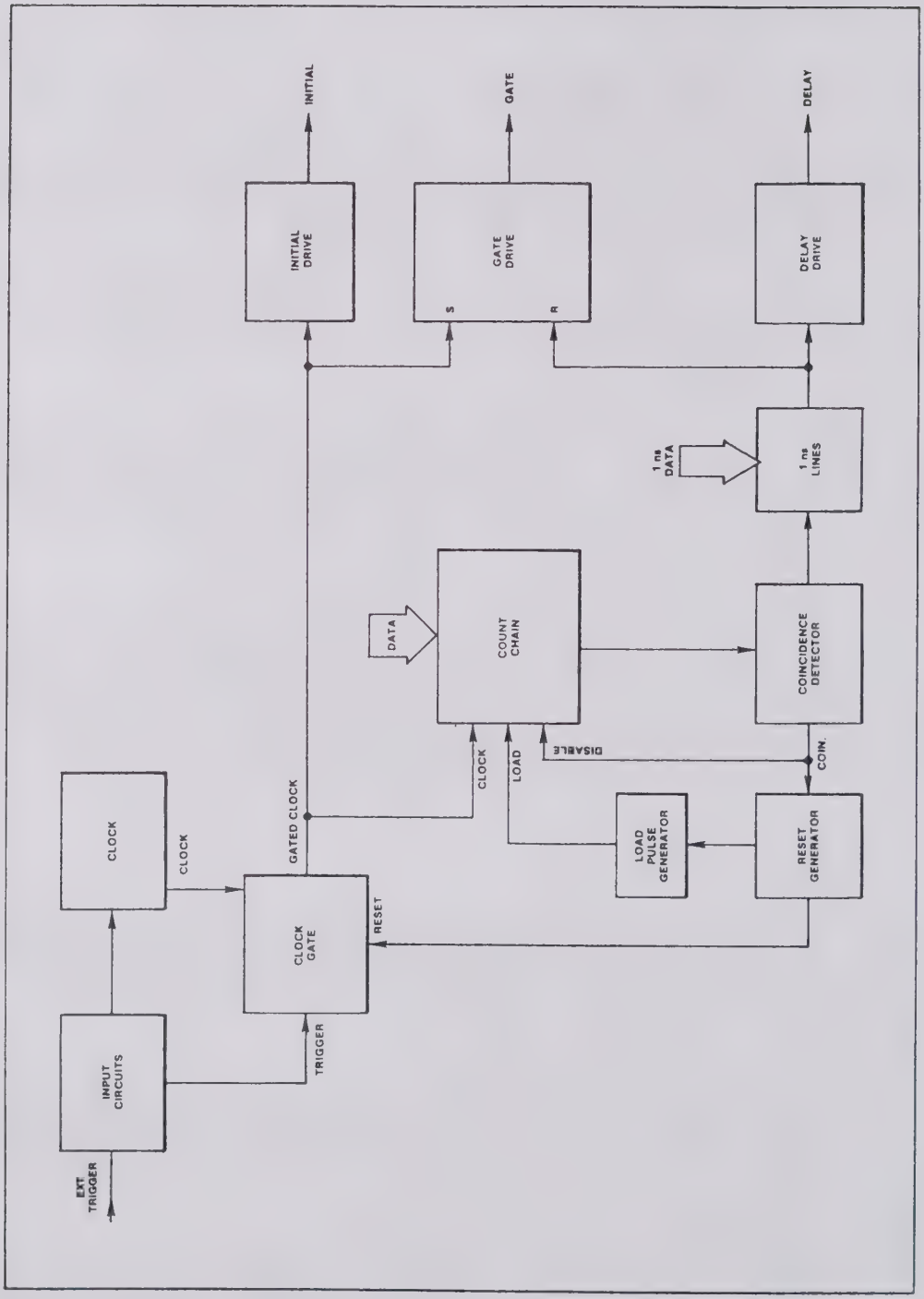


FIG. 3-2 Detailed Block Diagram of timing circuits.

3.2.3 CLOCK SYNCHRONIZING CIRCUITS AND OSCILLATOR (Fig. 3-1)

These circuits constitute a master oscillator which functions as master clock for the instrument's Timing circuits. The oscillator generates the 100 MHz clock signal, while the function of the Clock Synchronizing circuits is to provide outputs which are time-coherent with the Input Trigger pulses.

The TRIG signal from the Input Trigger Discriminator latches a one-shot. In turn, the one-shot stops the oscillator for 28 ns, after which the oscillator is restarted. It is this stop/restart sequence that initiates a digital timing cycle. This procedure ensures that the start of the timing cycle is always synchronous with the trigger input pulse leading edge, therefore, any indeterminacy between the input trigger and start of the count signal is eliminated.

Now the synchronized clock and trigger outputs are sent on to the Timing circuits.

3.2.4 TIMING CIRCUITS (Fig. 3-1, 3-2)

These circuits control the timing of the initial and delayed output pulses of the 7030A. The period between the initial pulse and delayed pulse establishes a time-interval (the magnitude being preset by the operator) which is measured in nanosecond increments. The gate pulse provides an operator with a convenient "window" between the initial and delayed pulses; its width being determined by the leading edges of the two pulses. Although the gate pulse is always triggered whenever the initial and delayed pulses are triggered, it is not significant or accurate if its width is less than 10 ns.

The Timing circuits produce a signal, the coincidence or end of count signal, which performs the actual delayed pulse triggering function. Triggering occurs when the count from the 10 ns decade counter reaches zero (0) or when the count is initially set at zero. In other words, the coincidence signal is the mechanism which ensures that the delayed pulse occurs precisely at the end (zero count) of the initial/delayed pulse interval. And finally, the Timing circuits generate a trigger disable signal which disables the trigger during the delay cycle.

From the Clock Synchronizing circuits, the first clock pulse generates the initial pulse and sets the beginning of the Gate pulse. The delayed pulse is also established by a clock pulse. However, the time at which it is actually triggered is determined by the number of 10 ns increments set into the count chain.

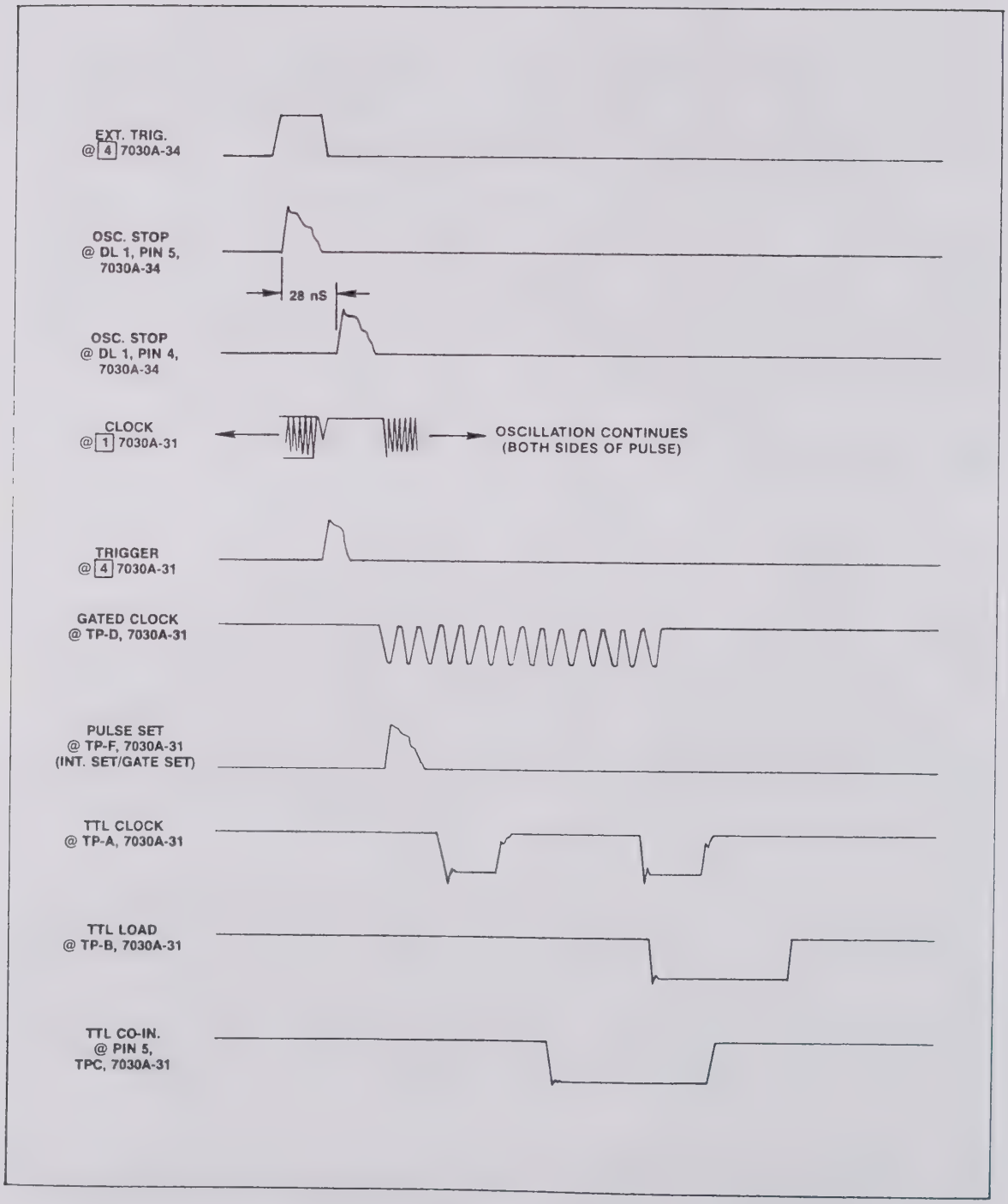


FIG. 3-3. Pulse Timing (Additional timing diagrams in Fig. 3-4)

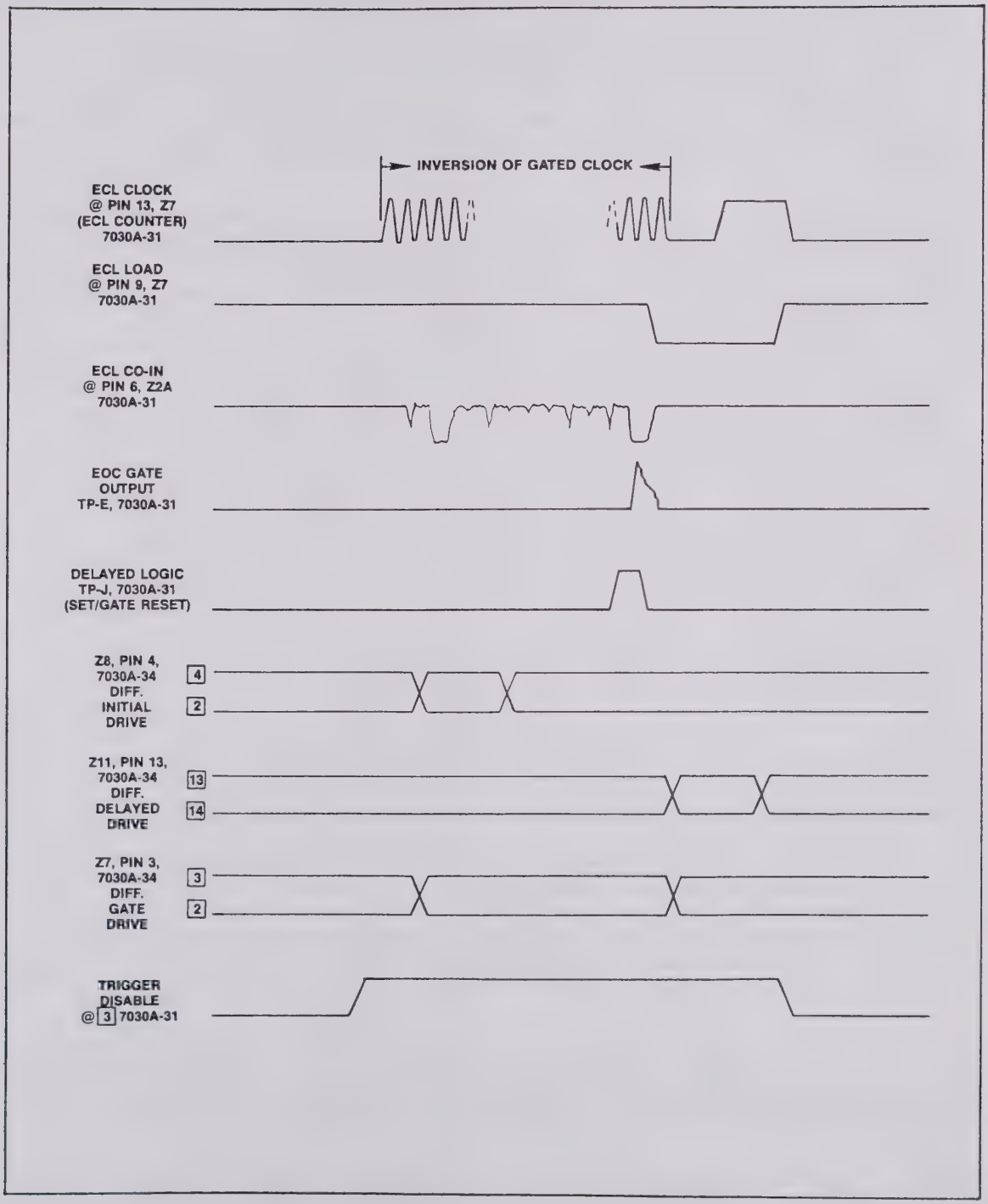

INVERSION OF GATED CLOCK
ECL CLOCK @ PIN 13, Z7 (ECL COUNTER) 7030A-31
ECL LOAD @ PIN 9, Z7 7030A-31
ECL CO-IN @ PIN 6, Z2A 7030A-31
EOC GATE OUTPUT TP-E, 7030A-31
DELAYED LOGIC TP-J, 7030A-31 (SET/GATE RESET)
Z8, PIN 4, 7030A-34 DIFF. INITIAL DRIVE
4
2
Z11, PIN 13, 7030A-34 DIFF. DELAYED DRIVE
13
14
Z7, PIN 3, 7030A-34 DIFF. GATE DRIVE
3
2
TRIGGER DISABLE @ 3 7030A-31

FIG. 3-4 Pulse Timing.

In other words, the interval between the initial and delayed pulses is the:

Initial pulse leading edge + "N" ns increments.

The settings are made either manually with the thumbwheel switches or automatically through the remote programming circuits.

The Initial/Delayed pulse interval also establishes the end of the gate pulse. Included within the Timing circuits is a subcircuit that permits a further breakdown of the 10 ns increments into 1 ns increments so that 1 ns resolution settings can be made.

The Timing circuits operate at both ECL and TTL levels. Those segments of the circuits directly affected by or related to the 100 MHz clock function are at ECL, because they must also operate at 100 MHz. The balance of the Timing circuits operates at TTL. The Coincidence signal also operates at both TTL and ECL levels. If the initial/delay pulse interval is greater than or equal to 100 ns, the signal operates in TTL. If the counting is done at less than 100 ns, the coincidence signal operates in ECL. Although TTL is slower, it offers the advantage of simpler circuit design with lower power consumption.

3.2.5 OUTPUT AMPLIFIERS (Fig. 3-1))

Model 7030A contains three output amplifiers. Each amplifier accepts a complementary (positive and negative) ECL-level input and all three amplifiers are identical in design.

The principal function of these amplifiers is as follows:

1. Boost the power of the three pulses by increasing the voltage and current levels.

2. Translate, or condition, the ECL signals so that the outputs are suitable for other instruments connected to the delay generators.

A direct ECL output would be very sensitive to loading and short circuiting (an ECL gate might be damaged). Moreover (as in the first function), without amplification and level translation, the TTL levels cannot be produced from an ECL gate.

Power is boosted from the ECL amplifier input of -0.7 volt to -1.7 volts, to an Initial and Delayed pulse output level of +5 volts into 50 ohms (Pos.) and -1 volt into 50 ohms (Neg.). The gate pulse output is boosted to +5 volts into 50 ohms.

Although these output signals (being higher) are neither specifically ECL or TTL, they are kept characteristically similar to those levels. The amplifier's design concept allows for the fact that some instruments, used with the 7030A, only accept TTL. Others trigger only with ECL. Still other instruments accept either ECL or TTL and trigger on either the positive or negative pulse slope. Thus, a user may want the availability of two outputs coincident with the same event.

The Model 7030A's outputs are short-circuit protected to prevent the output stage from being damaged if it is shorted to ground.

The Initial and Delayed pulse widths can be set with the WIDTH controls anywhere between 15 ns and 1 us. The GATE OUT has a width equal to the time between the Initial and Delayed pulses.

3.3 CIRCUIT DESCRIPTIONS

3.3.1 EXTERNAL TRIGGER DISCRIMINATOR (Schematic 7030A-34)

This circuit is shown in the upper left-hand quadrant of the schematic. Within the circuit is comparator Z1. The External Input Trigger enters the circuit at terminal 4 where it is attenuated by resistors R1, R2, and R3. These resistors also protect the comparator against damage from overvoltage. Feedback resistors R7 and R8 protect against multiple-triggering by generating hysteresis.

Potentiometer R803 permits selection of the input signal DC-level at which the comparator triggers. The potentiometer adjusts the comparison level of the inverting input at pin 3, Z1, and thus, adjusts the voltage at which the comparator switches. Complimentary outputs from pins 7 and 8, Z1, drive NOR gates Z6, pins 7 and 9 respectively. One of the signals, going to each gate, is delayed by an RC network comprised of either R30/C4 or R28/C3. This interconnection scheme permits the gating circuit to differentiate between the positive and negative edge of the incoming signal.

When the Slope switch, S801, is in the plus (+) position, the anode of diode CR1 is grounded. Thus, pin 6 of Z6B is at a high ECL level and the gate is disabled. At the same time, CR2 is reverse-biased and Z6A is enabled. Conversely, for negative slope selection, Z6A is disabled while Z6B is enabled.

3.3.2 MANUAL TRIGGER GENERATOR (Schematic 7030A-34)

This circuit is shown on the upper-center of the schematic. Gate Z4 forms an RS flip-flop debouncing circuit which changes state

each time the manual pushbutton, S802, is depressed. Outputs from the flip-flop, Z4, are fed to NOR gate, Z5, after being differentiated. The output, produced by wire-ORed gates, Z5 and Z6, initiates the oscillator stop signal sent to the Clock Synchronizing circuits.

3.3.3 CLOCK SYNCHRONIZING CIRCUITS (Schematic 7030A-34)

When a trigger signal is received, the positive transition of the trigger pulse at Z5, pin 6, sets the flip-flop composed of two of the Z5 gates whose outputs are pin 2 and pin 3. The output of Z5, pin 2, brings the input of Z4, pin 5 to a high level. This switches the differential outputs, pins 2 and 3. The differential outputs are transmitted to and disable the oscillator. At the time the trigger signal is received, it is also transmitted down a 28 ns delay. When this signal appears at the output of the delay, the flip-flop is reset and allows the oscillator to restart.

A third output from Z4, pin 4, is sent to the timing circuits to load new data into the DELAY memory/multiplexers. The remaining gate of Z5, pins 13 and 15, is an automatic reset for the clock-stop. On power up, if the output of Z5, pin 3, remains low (the set state) for more than 500 ns, C17 will charge up, bringing the output, pin 15, high and resetting the clock-stop flip-flop.

3.3.4 OSCILLATOR (Schematic 7030A-30)

A 100 MHz signal is generated in an oscillator circuit consisting of comparator Z1 and tuned circuit L1, C5. Coarse tuning is made with the adjustable slug in coil L1 and fine tuning is made by R64 (see schematic 7030A-34) located on the rear panel. The voltage selected by this potentiometer is applied to CR5 via pin 4 and causes the capacity of diode CR5 to change, thus tuning the oscillator.

The clock stop signal enters on pins 6 and 7, turning on Q1, Q2, and Q3. This applies a low impedance and fixed current to L1 via CR2, which stops the oscillator only for the short interval of the stop pulse. Oscillation starts again at the termination of this interval and will thus be phase coherent with the trigger.

3.3.5 OVEN (Schematic DR-15)

The oscillator is housed in an oven regulated at 60° C. This reduces the effect of ambient temperature changes on the frequency of oscillation. Thermistor R2, or amp Z1 and transistor Q1 determine the ambient of current applied to the internal heater coil in order to maintain a constant 60° C temperature.

3.3.6 TIMING CIRCUITS (See Figs. 3-3 & 3-4)

3.3.6.1 CLOCK GATE (Schematic 7030A-31)

Before the trigger signal enters the Timing circuits the signal level at TP-G, pin 5 of Z4, is high, thereby preventing the clock at pin 4 from passing through the gate. However, when the timing trigger is introduced, the state of the set/reset flip-flop, formed by Z8B and Z8C, changes and causes the level at TP-G to go low. Now the clock can pass through gate Z4A. At the end of each timing cycle, the reset circuitry generates a reset pulse at pin 9, Z8B, which resets the clock gate. TP-G again goes high and the clock is inhibited from passing gate Z4A. The resultant signal is a gated clock at TP-D. The total number of gated clock pulses is N plus 2 (N+2), where N represents the number of 10 nanosecond increments programmed into the instrument.

3.3.6.2 TRIGGER DISABLE (Schematic 7030A-31)

Gate Z8A ORs the complement of the clock gate at TP-G with the reset pulse from gate Z4C, thereby causing a high disable signal whenever any timing cycle is in progress. This signal is sent to the input circuits.

3.3.6.3 INITIAL LOGIC GENERATION (Schematic 7030A-31)

When the clock gate is opened by the timing trigger, the first cycle of the gated clock passes through gate Z2B to the test point TP-F. At this test point, the high-rising pulse activates the set/reset flip-flop (gates Z3A and Z3B) which returns the high signal to Z2B, pin 11, and blocks other clock pulses from passing the gate. At the end of the timing cycle, the flip-flop is reset by a reset signal emitted by pin 9 of Z3D. The resultant single pulse at TP-F is delayed by the four gates in the Z5 circuit.

Note that the number of gates in the logic path for the Initial pulse is equivalent to the number in the Delay Logic path. The purpose of this scheme is to reduce temperature effects and equalize signal propagation delays. The inverting input of comparator Z5, pins 4, 7, 10 and 13 are connected to a reference voltage which can be varied to alter the switching points of the gates. It is this arrangement that provides for a small adjustment range in the timing of the Initial logic signal at Z5B, pin 2, which brings the Initial and Delayed pulses into perfect coincidence at zero delay.

Transformation of the voltage change into a delay change occurs because the slope of an ECL signal is approximately one volt per three nanoseconds. Any level shift, therefore, results

in a corresponding change in the timing signal. Comparison voltage is attained by buffering the VBB output of Z5 with the unity-gain operational amplifier, Z10C. Resistors R4 and R56 then move the level slightly.

3.3.6.4 ECL COUNTER (Schematic 7030A-31)

The ECL decade counter, Z7, counts down from the number programmed by the 10 ns data generated by either the thumbwheel settings or by the remote programming circuits. The gate, Z4B, ORs the inverted gate clock with a with a signal from the reset circuitry and presents this signal to the counter clock input (Z7, pin 13). This switching procedure is necessary because the ECL counter requires a clock transition during the time it is loaded. Because the ECL counter outputs Q0 through Q3 are connected in a wire-ORed arrangement (i.e., counter outputs are all connected in parallel) an ECL low level occurs only when every tenth cycle of the gated clock generates this conditions. At which point, all the outputs are zero. This signal is the ECL coincidence signal which which enables the end of the count gate and TTL clock shaper.

3.3.6.5 TTL CLOCK SHAPER (Schematic 7030A-31)

The ECL coincidence signal is resynchronized to the gated clock by NOR gate Z2C. Translator Z1B shifts the gate output from an ECL to TTL level and also serves as a one-shot to widen the 5 ns pulses from the gated clock to 35 ns wide TTL clock pulses required by the TTL circuits.

3.3.6.6 TTL COUNTERS AND COINCIDENCE (Schematic 7030A-31, 7030A-32)

For delays greater than or equal to 100 ns the TTL counters Z15, Z16 and Z17 are used. The signals used to clock and load these counters and also the TTL COINcidence signal are signals which have been translated from ECL signals.

The counters are connected for ripple carry, where the carry from the LSD (Z15, pin 13) is connected to the next clock input, etc.

The counters are preset to the delay settings of 100 ns, 1 us, and 10 us decades. The condition of a nonzero count forces the MAX/MIN (pins 12) low, where they are NAND'ed and inverted by Z22 and fed to the Z16 ENABLE pin.

When a delay cycle is initiated, the counters count down from their present value, one after the other until all reach zero.

Then Z27, pin 6 goes low, asserting the TTL COIN (TTL Coincidence) and disabling the counters via Z22, pin 8, and counter pin 4.

The TTL COIN signal is translated to ECL by R24, R25, R26 and C35 for use by end-of-count gate Z2A (see 3.3.6.7).

3.3.6.7 END-OF-COUNT GATE (Schematic 7030A-31)

Z2A, found in the center of schematic 7030A-31, acts as the end-of-count detector. It uses signals from TTL COIN, ECL COIN and the gated CLOCK.

If a delay greater than or equal to 100 ns is entered, the TTL COIN signal at TP-C will be high, thus preventing output of an end-of-count pulse from Z2A, pin 3. In this event, the ECL counter Z7 (top of schematic) counts down the inverted version of the gated CLOCK and generates ECL COIN (see 3.3.6.4). This signal is conditioned by the TTL clock shaper circuit (see 3.3.6.5) and clocks the TTL counter until they reach zero. At this time the TTL COIN signal goes low and remains low until the next TTL LOAD cycle (See 3.3.6.8).

If a delay less than 100 ns was entered or TTL counters have reached zero, TTL COIN will be low. The ECL counter, Z7, will count down, and at zero generates ECL COIN (see 3.3.6.4) and the next low CLOCK cycle is passed through Z2A to TP-E for the end of cycle count. Meanwhile,, the ECL counter continues to count, going from 0 to 9, removing ECL COIN and preventing a second end of count signal.

3.3.6.8 RESET CIRCUITS (Schematic 7030A-31)

The reset one-shot, formed by gates Z3C and Z3D and delay line DL2, is triggered by the end-of-count pulse at TP-E. Gate Z4C ORs the one-shot's undelayed output at Z4C, pin 13, with a delayed output at pin 12. 14 ns later, the delayed reset output passes gate Z4B and goes to the clock input of the ECL counter. Result: A positive transition occurs on the ECL counter's clock pin while the load input at pin 9 is held low. As previously noted, this scheme provides the necessary gating procedure to load new data into the counter. The complement of the ECL load pulse is applied to pin 9, Z8B, thereby resetting the clock gate. This pulse causes the level at TP-G to return high and blocks further clock pulses from passing gate Z4A. A randomly occurring remote reset signal from the programming circuits can also trigger the reset circuit.

3.3.6.9 TTL LOAD SHAPER (Schematic 7030A-31)

Translator Z1D shifts the undelayed reset pulse at Z3, pin 9, from ECL to TTL levels. This gate performs a double role by also serving as a one-shot to widen the load pulse to roughly 40 ns. As a result, the TTL load pulse is applied to each of the TTL counters to load new data for the next timing cycle.

3.3.6.10 ONE NANOSECOND LINES (Schematic 7030A-31, 7030A-32)

The end-of-count signal at TP-E is buffered by gate Z6A and drives the 1 ns lines.

The output signal from Z6A drives two paths. The first is an undelayed path to Z9C. The second is a 2 ns delayed path to Z9B. When Z9C is selected, no incremental delay is added. But when Z9B is selected, a 2 ns delay is added. Again, the outputs of these two gates are wire-ORed to provide the drive for the next stage. In a like manner, gates Z11A and Z11D are used to select a 4 ns incremental delay. Z11B and Z11C are used to select the second 2 ns incremental delay. The output of the last two gates is combined to provide the delay logic signal at TP-J.

A similar selection process is employed for each delay line so that only the 1 ns line selection procedure need be described in detail. The inverting inputs of Z9A and Z9D are held either at an ECL high level (to disable) or at a level close to the -1.25 volt (VBB) center of the ECL logic range (to enable). At gate Z9A (which selects the 1 ns line), the level at the inverting input is adjustable over a narrow range so that the delay can be precisely set to 1 ns. The 1 ns adjustment trimmer, R5, is used for this purpose. It modifies the buffered VBB reference voltage provided by the unity-gain voltage follower, Z10D.

Drive signals that select the delay lines are derived from ECL type emitter follower outputs from Z13 (Schematic 7030A-32). When a high level is required to disable a gate, the emitter follower can easily drive the resistor from buffered VBB to pull the level to ECL high. However, when a gate is to be enabled, the emitter follower tries to drive the level to ECL low but is unable to do so, because the most negative voltage is close to VBB. The resultant signal is a back-biased emitter follower output and the selected gate input is allowed to stay close to the VBB level. Selection/disable functions occur in pairs - each time a gate is selected another is disabled. For example, when Z9A is enabled, Z9B is disabled. This procedure is predictable because all selection signals arrive in pairs (e.g., delay-line one and its complement).

3.3.6.11 GATE PULSE (Schematic 7030A-34, 7030A-31, 7030A-32)

Z7 on schematic 7030A-34 forms the set-reset gate pulse flip-flop. The initial logic signal at terminal 31 sets the flip-flop which is reset by a delay logic signal at terminal 32. Then, the resultant gate pulse is sent to the amplifier circuits. When the unit is in Calibration mode (switch on the back panel), the Gate Set and Gate Open will become high ECL level through CR6 and CR5 (Schematic 7030A-32). The Gate Open goes high to enable Z4 (Schematic 7030A-31) and allow the 100 MHz oscillator to clock the first ECL counter Z7 and TTL clock shaper Z1B. The resultant 10 MHz signal at TTL level now clocks the TTL counter chain (Schematic 7030A-32) and is divided to 1 MHz by the first counter Z16. The signal is translated by R64, 65, 66 Q1 and Q2 to an ECL signal and transmitted to Z7 (Schematic 7030A-34) through a twisted pair.

3.3.7 OUTPUT AMPLIFIERS (Schematic 7030A-36)

Note that the following discussion of the initial pulse amplifier may also be used as a model for the delayed pulse and gate amplifier operation.

The differential initial drive pulse is received from the timing circuits. A differential amplifier formed by Q1 and Q2 amplifies the ECL level signal, while Q1 and Q2 collector signals drive a second differential amplifier, Q3 and Q4.

The collector signals from Q3 and Q4 become the negative and positive initial output pulses which drive emitter followers Q5 and Q7.

Transistor Q7 derives its steady-state collector current from transistor Q6. In turn, Q6 provides short-circuit protection for the output device. The output current is limited by the current source comprised of CR1, R16, R17, R20 and Q6.

The pulse may be varied from 15 ns to 1 us using the two Width control knobs on the front panel; one is for Initial Pulse adjustment, the other, for Delayed Pulse. The Initial Pulse Width control varies the Initial Positive and Negative widths simultaneously. The Delayed Pulse Width control simultaniously varies the Delayed Positive and Negative widths.

SECTION 4

MAINTENANCE

4.1 INTRODUCTION

This section describes maintenance and calibration procedures for the Model 7030A. Before attempting to troubleshoot and repair a unit, refer to the appropriate information in Section 3 for general and detailed circuit description.

The great majority of 7030A's components can be replaced with standard items stocked by the local major distributors. The few exceptions include the oven assembly and glass piston inductors which are available from Berkeley Nucleonics Corporation under part numbers noted in Section 5.

4.2 PREVENTIVE MAINTENANCE

The least costly and time-saving approach to reliable and accurate operation of the Model 7030A is through timely application of a preventive maintenance procedure. This includes periodic visual inspection, cleaning of controls and internal circuit boards and recalibration, if necessary. The interval for maintenance activities is largely dictated by the operating environment as well as the user's established maintenance practices and philosophy.

If no established instrument maintenance schedule is currently being followed, Berkeley Nucleonics suggests following a regular schedule of timely inspection and maintenance at least once a year.

Periodically the delay generator should be inspected and cleaned of dust and grit using a jet of compressed air, vacuum or a suitable brush. Discolored components and those showing physical damage and deterioration should be identified and replaced. Sources which cause discoloration should be located and corrected.

4.3 CORRECTIVE MAINTENANCE

If there are no outputs after turning the unit on, be sure the instrument is connected to an active power source of the correct voltage. Next check to see that the rear panel switch is in the OPERATE position.

Other problems may be analyzed and corrected by referring to circuit descriptions, schematics and calibration procedures.

SECTION 5

CALIBRATION

5.1 CALIBRATION

5.1.1 BASIC REQUIREMENTS/TEST EQUIPMENT

----------NOTE----------
Model 7030A should be at normal operating temperature for at least 1 hour before starting precision calibration. Adjustments to the DC power supplies, however, may be started five minutes after turn-on.

The steps to calibrate the instruments must be followed in the order given. Calibration of the Model 7030A requires attention to four principal elements whose adjustment is critical to accurate instrument operation. These are the following:

A. Power supplies
B. Clock frequency
C. Zero Delay coincidence; Initial Pulse (leading edge) to Gate coincidence; Delayed Pulse (leading edge) to Gate coincidence
D. Least significant (1 ns) decade

With the exception of the optional Hewlett-Packard Time Interval Counter, the following test equipment or its equivalent is essential for accurate calibration of the Model 7030A:

Oscilloscope: Tektronix Model 485 (with 350 MHz bandwidth, 1 ns time division resolution).

X 1 Oscilloscope Probe.

Digital Multimeter/Voltmeter (DVM): Fluke Model 8022A (or other DVM with 3.5 digits).

Frequency Counter with 1 Hz resolution.

Digital Delay Generator: BNC Model 7050 (or other pulse source having crystal controlled, low jitter output pulses with 5 ns or less rise time and 10 ns delay resolution. A 100 MHz clock is also desirable.

Optional: Hewlett-Packard Model HP5370A Universal Time Interval Counter.

5.1.2 POWER SUPPLIES

Using a DVM, adjust R57 (PCB 7030A-4) for a voltage of +6.00 volts at board connection #19 and adjust R59 for a voltage of -5.20 volts at board connection #18.

Monitor all power supplies to ensure operation at specified DC voltage levels and to ensure acceptable AC ripple and oscillation components. In all cases, AC ripple should be less than 5 mV peak when viewed with a 20 MHz bandwidth oscilloscope. The power supplies should never exhibit any high frequency oscillation.

5.1.3 OSCILLATOR ADJUSTMENT

Connect a counter to the GATE OUT connector and switch S901 on the rear panel to the OSC CAL position. The frequency output of the Gate connector should be 1 MHz ($\pm 5 \times 10^{-6}$). If this output is not within limits, adjust R64 (Fine Freq. Adj.) which is accessible through the hole in the rear panel just above the CAL/Operate switch. If this adjustment does not have sufficient range, use the coarse adjustment screw which is accesible through a hole in the top of the oscillator can. Reset the Fine Adjustment to the center of its 15 turns total range prior to making the coarse adjustment. It is advisable to use a plastic alignment tool so as not to disturb the thermal equilibrium in the oven. The adjustment end of the coarse adjust is similar to that of the Fine Adjustment.

---NOTE---

Return the rear panel switch to the OPERATE position.

5.1.4 OSCILLATOR START ADJUSTMENT (PC Board 7030A-4)

a) Trigger 7030A from a 7050 with DELAY set at 10 us and MODE set at PERIOD for a 100 KHz pulse rate.

b) Trigger the oscilloscope from 7030A Positive Delayed Pulse ("+" slope).

c) Display 7050 100 MHz "clock out" on the oscilloscope (model 485). Set to 1 ns sweep speed and 200 mV per division sensitivity)) so that the 50% point of the positive transition crosses the center graticules.

d) Sweep (locally or remotely) the 10 ns decade of the 7030A. Adjust R61 for minimum deviation of displayed

clock at center graticules (50% points); this should be less than 0.6 ns peak-to-peak.

5.1.5 PULSE COINCIDENCE

The Initial and Delayed output pulses are adjusted so that the 50% level point of each of the four leading edges is coincident within 100 ps when the instrument DELAY is set to zeros. When viewing these pulses on the oscilloscope, certain precautions must be taken to avoid error. First, the oscilloscope must have a real or effective bandwidth of at least 350 MHz (1 ns rise time) in order that bandwidth distortion of the nominally 3 ns rise time pulse transition is minimized. In addition, timing errors caused by oscilloscope channel imbalances and cable length differences must be carefully avoided. RG-58, 50 ohm coaxial cable has a propagation speed of approximately 120 ps per inch. Therefore, cable length differences of as little as one inch will cause errors that exceed the specified accuracy of the Model 7030A. Before proceeding, please see Para. 2.1.3 (Cables, Attenuators and Oscilloscopes).

a) Center R4 (PC board 7030A-2).

b) Center R8 on all three PC boards 7030A-5 (Initial, Delay and Gate Amplifier boards).

c) Trigger 485 and 7030A from 7050 (1 us, period mode).

d) Set 485 A sweep for 50 ns per division, B sweep 1 ns per division; set 485 for 1 Volt per division. Set to alternate A and B sweep.

e) Set 7030A for 100 ns delay.

f) Display Gate Out leading edge on 485 A sweep and adjust vertical sweep to display 10 and 90% points with 50% point crossing center graticule; display trailing edge of Gate Out on 485 B sweep and set so that the trailing edge crosses center graticules. Using same cable and scope channel display Delayed Pulse (100 ns Width) and vary vertical setting to display 10 and 90% points with 50% points crossing center graticule. Adjust R8 on Delay Amp board to align 50% point of Delay Pulse to center graticule.

g) Repeat above for Initial to leading edge of Gate Out (R8 on Gate Amp board can also be used for this).

h) Set 7030A for zero Delay and adjust R4 (marked To) on PC board 7030A-2 for coincidence of leading edge of Initial to Delay pulses at 50% points.

i) Display positive Initial as above for 50% points to cross center graticules (B sweep); with the same cable display negative Initial Pulse and set to view 10, 50 and 90% points (50% point crossing center horizontal graticule) and adjust C7 so leading edge crosses center graticules.

j) Repeat item "i" for positive to negative Delayed Pulse alignment.

5.1.6 LEAST SIGNIFICANT DECADE ADJUSTMENT

The 1 ns resolution of the least significant decade is attained through the use of four fixed-length coaxial delay lines. These delay lines have nominal lengths of 1 ns, 2 ns, 4 ns and 2 ns. Various combinations of these lines are used to produce a range of 0 to 9 ns delay in 1 ns steps.

The effective delay of each of the four coaxial lines is electrically adjusted by four independent variable resistors to obtain the ±100 ps tolerance specified. The adjustments are identified as follows:

1 ns - R5
2 ns(A) - R7
4 ns - R8
2 ns(B) - R9

When making these adjustments, first note the accuracy of each delay from 1 to 9 ns. In all cases, these accuracies are measured relative to 0 ns delay. If any delay is not within the specified ±100 ps tolerance, it may be adjusted by the appropriate resistor(s), referring to the table below. Whenever one of the resistors is adjusted, it will be necessary to check all other delays affected by that adjustment. In some cases it may be necessary to compromise between two or more delays to achieve the +100 ps accuracy throughout.

DELAY SETTING	COAX LINE COMBINATION	ADJUSTING RESISTORS
1 ns	1 ns only	R5
2 ns	2 ns only	R7
3 ns	1 ns and 2 ns	R5 and R7
4 ns	4 ns only	R8
5 ns	4 ns and 1 ns	R8 and R5
6 ns	4 ns and 2 ns	R8 and R7
7 ns	4 ns, 2 ns and 1 ns	R8, R7 and R5
8 ns	4 ns, 2 ns and 2* ns	R8, R7 and R9
9 ns	4 ns, 2 ns, 2* ns and 1 ns	R8, R7, R5 and R9

2* refers to the 2 ns line in the second set of delay lines.

For example, suppose that 3 ns delay was found to be out of tolerance. Adjustment of this delay involves R5 (1 ns) and R7 (2 ns). Thus, all other delays which are affected must be taken into account. These are 1 ns, 2 ns, 5 ns, 6 ns, 7 ns, 8 ns and 9 ns. By experimenting with the four adjustments, it will be possible to achieve a compromise by which each delay from 1 ns to 9 ns is within $\pm$100 ps of its nominal value, measured with respect to 0 ns delay.

SECTION 5

PARTS LISTS AND SCHEMATICS

ABBREVIATIONS

cer	ceramic	μH	microhenry
comp	composition carbon	μF	microfarad
elec	electrolytic, metal case	pF	picofarad
mic	mica	pos	positions
myl	mylar	sel	selected value
K	kilohm	tan	tantalum
KV	kilovolt	V	working volts DC
M	megohm	var	variable
m	milli	W	watts
MF	metal film	ww	wirewound

---------- NOTE ----------

The last number after each part description is the BERKELEY NUCLEONICS part number for re-ordering.

INPUT/OUTPUT BOARD 7030A-4				649-059
C1	0.05 μF	cer	25 V	110-019
C2	0.05 μF	cer	25 V	110-019
C3	33 pF	mic	500 V	112-002
C4	33 pF	mic	500 V	112-002
C5	0.05 μF	cer	25 V	110-019
C6	0.05 μF	cer	25 V	110-019
C7	0.05 μF	cer	25 V	110-019
C8	0.05 μF	cer	25 V	110-019
C9	10 μF	tan	15 V	122-016
C10	270 pF	mic	500 V	112-009
C11	0.05 μF	cer	25 V	110-019
C12	10 μF	tan	15 V	122-016
C13	270 pF	mic	500 V	112-009
C14	0.05 μF	cer	25 V	110-019
C15	0.05 μF	cer	25 V	110-019
C16	33 pF	mic	500 V	112-002
C17	0.001 μF	cer	1 KV	110-011
C18	10 μF	tan	15 V	122-016
C19	10 μF	tan	15 V	122-016
C20	33 μF	tan	25 V	122-015
C21	0.05 μF	cer	25 V	110-019
C22	33 μF	tan	25 V	122-015
C23	0.05 μF	cer	25 V	110-019
C24	0.05 μF	cer	25 V	110-019
C25	0.05 μF	cer	25 V	110-019
C26	0.05 μF	cer	25 V	110-019
C27	0.05 μF	cer	25 V	110-019
C28	0.05 μF	cer	25 V	110-019
C29	0.05 μF	cer	25 V	110-019
C30	0.05 μF	cer	25 V	110-019
C31	33 μF	tan	25 V	122-015
C32	33 μF	tan	25 V	122-015
C33	10 μF	tan	15 V	122-016
C34	10 μF	tan	15 V	122-016
C35	10 μF	tan	15 V	122-016
C36	10 μF	tan	15 V	122-016

CR1	1N4152	411-004
CR2	1N4152	411-004
CR3	1N5234B	412-010
CR4	HP5082-2835	415-004
CR5	Not Used	
CR6	HP5082-2835	415-004
CR7	1N4152	411-004
CR8	1N4005	410-003
CR9	1N4005	410-003
CR10	1N4005	410-003
CR11	1N4005	410-003
CR12	1N4005	410-003
CR13	1N4005	410-003

DL1	ECLDM-35 (Logic Delay)	316-019

R1	390 Ω	1/4 W	comp	5%	213-391
R2	56 Ω	1/2 W	comp	5%	212-563
R3	91 Ω	1/4 W	comp	5%	213-910
R4		None			
R5	15 K	1/4 W	comp	5%	213-153
R6	1.2 K	1/4 W	comp	5%	213-122
R7	3.3 K	1/4 W	comp	5%	213-332
R8	120 Ω	1/4 W	comp	5%	213-121
R9		None			
R10	1K	1/4 W	comp	5%	213-102
R11	5.6 K	1/4 W	comp	5%	213-562
R12	10 K	1/4 W	comp	5%	213-103
R13	51 Ω	1/4 W	comp	5%	213-510
R14	2.37 K	1/4 W	MF	1%	222-043
R15	1 K		var		244-020
R16	82 Ω	1/4 W	comp	5%	213-820
R17	130 Ω	1/4 W	comp	5%	213-131
R18	10 K	1/4 W	comp	5%	213-103
R19	470 Ω	1/4 W	comp	5%	213-471
R20	1 K	1/4 W	comp	5%	213-102

. . . continued

R21	51 Ω	1/4 W	comp	5%	213-510
R22	2.37 K	1/4 W	comp	5%	213-242
R23	1 K		var		244-020
R24	68 Ω	1/4 W	comp	5%	213-680
R25	82 Ω	1/4 W	comp	5%	213-820
R26	130 Ω	1/4 W	comp	5%	213-131
R27	390 Ω	1/4 W	comp	5%	213-391
R28	390 Ω	1/4 W	comp	5%	213-391
R29	270 Ω	1/4 W	comp	5%	213-271
R30	390 Ω	1/4 W	comp	5%	213-391
R31	270 Ω	1/4 W	comp	5%	213-271
R32	10 K	1/4 W	comp	5%	213-103
R33	10 K	1/4 W	comp	5%	213-103
R34	390 Ω	1/4 W	comp	5%	213-391
R35	68 Ω	1/4 W	comp	5%	213-680
R36	390 Ω	1/4 W	comp	5%	213-391
R37	1 K	1/4 W	comp	5%	213-102
R38	390 Ω	1/4 W	comp	5%	213-391
R39	390 Ω	1/4 W	comp	5%	213-391
R40	390 Ω	1/4 W	comp	5%	213-391
R41	1 K	1/4 W	comp	5%	213-102
R42	390 Ω	1/4 W	comp	5%	213-391
R43	390 Ω	1/4 W	comp	5%	213-391
R44	390 Ω	1/4 W	comp	5%	213-391
R45	390 Ω	1/4 W	comp	5%	213-391
R46	47 Ω	1/4 W	comp	5%	213-470
R47	47 Ω	1/4 W	comp	5%	213-470
R48	390 Ω	1/4 W	comp	5%	213-391
R49	270 Ω	1/4 W	comp	5%	213-271
R50	47 Ω	1/4 W	comp	5%	213-470
R51	47 Ω	1/4 W	comp	5%	213-470
R52	390 Ω	1/4 W	comp	5%	213-391
R53	240 Ω	1/4 W	comp	5%	213-241
R54	240 Ω	1/4 W	comp	5%	213-241
R55	249 Ω	1/4W	MF	1%	222-011
R56	909 Ω	1/4 W	MF	1%	222-016
R57	100 Ω		var		244-019
R58	249 Ω	1/4 W	MF	1%	222-011
R59	100 Ω		var		244-019
R60	649 Ω	1/4 W	MF	1%	222-038
R61	500 Ω		var		244-004
R62	470 Ω	1/4 W	comp	5%	213-471
R64	1 K		var		244-026
R65	1 K	1/4 W	MF	1%	222-039

Z1	AM685	440-033
Z2	LM337T	440-125
Z3	LM317T	440-124
Z4	MC10212	440-078
Z5	MC1662	440-072
Z6	MC10212	440-078
Z7	MC10212	440-078
Z8	MC10212	440-078
Z9	MC10216	440-069
Z10	LM348	440-068
Z11	MC10212	440-078

Gate	Socket, 16-pin	621-022
Initial	Socket, 16-pin	621-022
Delay	Socket, 16-pin	621-022

OUTPUT AMPLIFIER 7030A-5 649-057

C1	0.05 μF	cer	25 V	110-019
C2	0.05 μF	cer	25 V	110-019
C3	0.05 μF	cer	25 V	110-019
C4	0.05 μF	cer	25 V	110-019
C5	0.05 μF	cer	25 V	110-019
C6	0.05 μF	cer	25 V	110-019
C7	4-30 pF	var		130-005
C8	10 μF	tan	15 V	122-016
C9	0.05 μF	cer	25 V	110-019
C10	10 μF	tan	15 V	122-016
C11	0.05 μF	cer	25 V	110-019
C12	0.05 μF	cer	25 V	110-019
C13	0.05 μF	cer	25 V	110-019

CR1	1N5234B	412-010
CR2	1N5231B	412-009
CR3	5082-2811	415-003
CR4	5082-2811	415-003
L1	0.47 μH	311-002
L2	5.6 μH	311-003
Q1	2N4208	430-052
Q2	2N4208	430-052
Q3	2N5836	430-055
Q4	2N5836	430-055
Q5	MM4049	430-056
Q6	2N2905	430-049
Q7	LT1001	430-046

R1	300 Ω	1/4 W	comp	5%	213-301
R2	180 Ω	1/4 W	comp	5%	213-181
R3	300 Ω	1/4 W	comp	5%	213-301
R4	300 Ω	1/4 W	comp	5%	213-301
R5	150 Ω	1/2 W	comp	5%	212-151
R6	51 Ω	1/4 W	comp	5%	213-510
R7	51 Ω	1/4 W	comp	5%	213-510
R8	50 Ω		var		244-018
R9	180 Ω	1/4 W	comp	5%	213-181
R10	62 Ω	1/4 W	comp	5%	213-620
R11	1 K	1/4 W	comp	5%	213-102
R12	620 Ω	1/4 W	comp	5%	213-621
R13	560 Ω	1/4 W	comp	5%	213-561
R14	51 Ω	1/4 W	comp	5%	213-510
R15	470 Ω	1/2 W	comp	5%	212-471
R16	82 Ω	1/2 W	comp	5%	212-820
R17	82 Ω	1/2 W	comp	5%	212-820
R18	51 Ω	1/4 W	comp	5%	213-510
R19	390 Ω	1/4 W	comp	5%	213-391
R20	470 Ω	1/4 W	comp	5%	213-471

Header, R/angle, 16-pin	620-004
Pad, Insulator (Q1-Q5)	509-003
Pad, Insulator (Q6, Q7)	509-004
Buss Bar 2"	629-002
Insulator, Buss Bar 2"	509-012

LOGIC BOARD 7030A-2				649-064
C1	33 μF	tan	25 V	122-015
C2	0.05 μF	cer	25 V	110-019
C3	0.05 μF	cer	25 V	110-019
C4	0.05 μF	cer	25 V	110-019
C5	0.05 μF	cer	25 V	110-019
C6	0.05 μF	cer	25 V	110-019
C7	0.05 μF	cer	25 V	110-019
C8	0.05 μF	cer	25 V	110-019
C9	0.05 μF	cer	25 V	110-019
C10	0.05 μF	cer	25 V	110-019
C11	0.05 μF	cer	25 V	110-019
C12	0.05 μF	cer	25 V	110-019
C13	0.05 μF	cer	25 V	110-019
C14	0.05 μF	cer	25 V	110-019
C15	0.05 μF	cer	25 V	110-019
C16	0.05 μF	cer	25 V	110-019
C17	0.05 μF	cer	25 V	110-019
C18	0.05 μF	cer	25 V	110-019
C19	33 μF	tan	25 V	122-015
C20	0.05 μF	cer	25 V	110-019
C21	0.05 μF	cer	25 V	110-019
C22	0.05 μF	cer	25 V	110-019
C23	0.05 μF	cer	25 V	110-019
C24	0.05 μF	cer	25 V	110-019
C25	0.05 μF	cer	25 V	110-019
C26	0.05 μF	cer	25 V	110-019
C27	0.05 μF	cer	25 V	110-019
C28	0.05 μF	cer	25 V	110-019
C29	0.05 μF	cer	25 V	110-019
C30	0.05 μF	cer	25 V	110-019
C31	0.05 μF	cer	25 V	110-019
C32	33 μF	tan	25 V	122-015
C33	33 μF	tan	25 V	122-015
C34	0.05 μF	cer	25 V	110-019
C35	10 pF	mic	500 V 5%	112-016
C36	0.05 μF	cer	25 V	110-019
C37	56 pF	mic	500 V 5%	112-022
C38	56 pF	mic	500 V 5%	112-022
C39	0.001 μF	cer		110-011
C40	0.001 μF	cer		110-011
C41	82 pF	mic	500 V 5%	112-020
C42	10 pF	mic	500 V 5%	112-016
C43	0.001 μF	cer	1 K 10%	110-011
C44	0.001 μF	cer	1 K 10%	110-011
C45	0.001 μF	cer	1 K 10%	110-011
C46	0.001 μF	cer	1 K 10%	110-011
C47	0.001 μF	cer	1 K 10%	110-011
C48	0.001 μF	cer	1 K 10%	110-011
C49	10 pF	mic	500 V 5%	112-016
C50	0.05 μF	cer	25 V	110-019
C51	0.05 μF	cer	25 V	110-019
CR1		1N4005		410-003
CR2		1N4005		410-003
CR3		1N5713		415-003
CR4		1N5713		415-003
CR5		1N4152		411-004
CR6		1N4152		411-004
CR7		1N4152		411-004
CR8		1N4152		411-004
CR9		Not Used		
CR10		Not Used		
CR11		1N4152		411-004
CR12		1N4152		411-004
CR13		1N4152		411-004
CR14		1N4152		411-004
DL1	2 ns			316-009
DL2	ECLDM-35			316-019
DL3	1 ns (Ref Dwg. 7065-29)			316-010
DL4	2 ns (Ref Dwg. 7065-29)			316-011
DL5	4 ns (Ref Dwg. 7065-29)			316-012
DL6	2 ns (Ref Dwg. 7065-29)			316-011
J1	Connector, 36-pin Amphenol			619-001
J3	Socket, 16-pin w/clip			621-010
J4	Socket, 16-pin w/clip			621-010
L1	0.22 μH			311-004
Q1	MPS3646			430-027
Q2	MPS3646			430-027
Q3	MPS3646			430-027
R1	470	5 Resistor SIP		223-011
R2	470	5 Resistor SIP		223-011
R3	81/130	4 Pair Resistor SIP		223-012
R4	5 K	var		244-038
R5	5 K	var		244-038
R6	180	5 Resistor SIP		223-009
R7	5 K	var		244-038
R8	5 K	var		244-038
R9	5 K	var		244-038
R10	180	5 Resistor SIP		223-009
R11	1 K	5 Resistor SIP		223-010
R12	130 Ω	1/4 W	comp 5%	213-131
R13	82 Ω	1/4 W	comp 5%	213-820
R14	82 Ω	1/4 W	comp 5%	213-820
R15	130 Ω	1/4 W	comp 5%	213-131
R16	68 Ω	1/4 W	comp 5%	213-680
R17	470 Ω	1/4 W	comp 5%	213-471
R18	270 Ω	1/4 W	comp 5%	213-271
R19	470 Ω	1/4 W	comp 5%	213-471
R20	39 Ω	1/4 W	comp 5%	213-390
R21	270 Ω	1/4 W	comp 5%	213-271
R22	82 Ω	1/4 W	comp 5%	213-131
R23	270 Ω	1/4 W	comp 5%	213-271
R24	249 Ω	1/4 W	MF 1%	222-011
R25	422 Ω	1/4 W	MF 1%	222-013
R26	499 Ω	1/4 W	MF 1%	222-014
R27	390 Ω	1/4 W	comp 5%	213-391
R28	82 Ω	1/4 W	comp 5%	213-820
R29	82 Ω	1/4 W	comp 5%	213-820
R30	150 Ω	1/4 W	comp 5%	213-151

. . . continued

Logic Board (continued)

R31	56 Ω	1/4 W	comp	5%	213-560
R32	2.7 K	1/4 W	comp	5%	213-272
R33	14 K	1/4 W	MF	1%	222-043
R34	180 Ω	1/4 W	comp	5%	213-181
R35	270 Ω	1/4 W	comp	5%	213-271
R36	2.7 K	1/4 W	comp	5%	213-272
R37	150 Ω	1/4 W	comp	5%	213-151
R38	56 Ω	1/4 W	comp	5%	213-560
R39	1.5 K	1/4 W	comp	5%	213-152
R40	130 Ω	1/4 W	comp	5%	213-131
R41	82 Ω	1/4 W	comp	5%	213-820
R42	14 K	1/4 W	MF	1%	222-043
R43	14 K	1/4 W	MF	1%	222-043
R44	130 Ω	1/4 W	comp	5%	213-131
R45	82 Ω	1/4 W	comp	5%	213-820
R46	82 Ω	1/4 W	comp	5%	213-820
R47	130 Ω	1/4 W	comp	5%	213-131
R48	130 Ω	1/4 W	comp	5%	213-131
R49	82 Ω	1/4 W	comp	5%	213-820
R50	14 K	1/4 W	MF	1%	222-043
R51	Not Used				
R52	Not Used				
R53	130 Ω	1/4 W	comp	5%	213-131
R54	82 Ω	1/4 W	comp	5%	213-820
R55	178 Ω	1/4 W	MF	1%	222-036
R56	28 K	1/4 W	MF	1%	222-024
R57	10 K	1/4 W	comp	5%	212-103
R58	10 K	1/4 W	comp	5%	212-103
R59	1 K	1/4 W	comp	5%	212-102
R60	10 K	1/4 W	comp	5%	212-103
R61	22 K	1/4 W	comp	5%	212-223
R62	10 K	1/4 W	comp	5%	212-103
R63	10 K	1/4 W	comp	5%	212-103
R64	1.21 K	1/4 W	MF	1%	222-072
R65	845 Ω	1/4 W	comp	5%	222-062
R66	499 Ω	1/4 W	MF	1%	222-014
R67	499 Ω	1/4 W	MF	1%	222-014
R68	845 Ω	1/4 W	MF	1%	222-062
R69	1.21 K	1/4 W	MF	1%	213-122
R70	22 K	1/4 W	comp	5%	213-223
R71	Not Used				
R72	Not Used				
R73	3.3 K	1/4 W	comp	5%	213-332
R74	220 Ω	1/4 W	comp	5%	213-221
R75	Not Used				
R76	10 K	1/4 W	comp	5%	213-103
R77	10 K	1/4 W	comp	5%	213-103
R78	1 K	1/4 W	comp	5%	213-102
R79	100 Ω	1/4 W	comp	5%	213-101
R80	82 Ω	1/4 W	comp	5%	213-820
R81	130 Ω	1/4 W	comp	5%	213-131
R82	100 Ω	1/4 W	comp	5%	213-101
R83	10 K	1/4 W	comp	5%	213-103
R84	1 K	1/4 W	comp	5%	213-102

Z1	10125	440-041
Z2	10106	440-046
Z3	10102	440-045
Z4	10105	440-044
Z5	10515	440-079
Z6	10105	440-044
Z7	10137	440-048
Z8	10105	440-044
Z9	10515	440-079
Z10	LM348	440-068
Z11	10515	440-079
Z12	10124	440-070
Z13	10124	440-070
Z14	7402	440-074
Z15	74190	440-036
Z16	74190	440-036
Z17	74190	440-036
Z18	74LS298	440-107
Z19	74LS298	440-107
Z20	74LS298	440-107
Z21	74LS298	440-107
Z22	74S20	440-128
Z23	74LS240	440-129
Z24	74LS240	440-129
Z25	74LS240	440-129
Z26	74LS298	440-107
Z27	74S00	440-038
Z28	74LS08	440-096

Bus Bar 4"	629-004
Bus Bar 3"	629-003
Bus Bar 1"	629-001
Bus Bar Insulator, 4"	509-014
Bus Bar Insulator, 3"	509-013
Bus Bar Insulator, 1"	509-011

OSCILLATOR BOARD 649-050

C1	0.01 μF	cer	16 V	20%	110-021
C2	47 pF	mic	500 V	5%	112-003
C3	10 pF	cer	1 KV	±.5%	110-002
C4	0.01 μF	cer	16 V	20%	110-021
C5	10 pF	cer	1 KV	±5%	110-023
C6	0.01 μF	cer	16 V	20%	110-021
C7	0.01 μF	cer	16 V	20%	110-021
C8	0.01 μF	cer	16 V	20%	110-021
C9	0.01 μF	cer	16 V	20%	110-021

CR1	1N5231B	412-009
CR2	1N5713	415-003
CR3	1N5713	415-003
CR4	1N5713	415-003

L1	0.22 μH	var	308-001

. . . continued

Oscillator Board (continued)

R1	120 Ω	1/4 W	comp	5%	213-121
R2	1.2 K	1/4 W	comp	5%	213-123
R3	390 Ω	1/4 W	comp	5%	213-391
R4	390 Ω	1/4 W	comp	5%	213-391
R5	51 Ω	1/4 W	comp	5%	213-510
R6	330 Ω	1/4 W	comp	5%	213-331
R7	470 Ω	1/4 W	comp	5%	213-471
R8	1.2 K	1/4 W	comp	5%	213-123
R9	560 Ω	1 W	comp	5%	211-561
R10	39 Ω	1/4 W	comp	5%	213-390
R11	1.2 K	1/4 W	comp	5%	213-123
R12	390 Ω	1/4 W	comp	5%	213-391
R13	1 M	1/4 W	comp	5%	213-105

P5	Connector, 15-pin male	619-003
Q1	2N3646	430-027
Q2	2N3646	430-027
Q3	2N3646	430-027
T1	Ferrite core w/2 turns of wire, twisted pair	318-003
Z1	AM685	440-033

THUMBWHEEL SWITCH BOARD 649-063

J3	Socket, 16-pin w/clip	621-010
J4	Socket, 16-pin w/clip	621-010
S1 thru S5	Switch, Thumbwheel	610-021
	Brackets, end	531-015
	Strap #5	531-011

OSCILLATOR INTERFACE 7030A-6 649-083

C1	0.05 μF	cer	25 V	110-019
C2	0.05 μF	cer	25 V	110-019
C3	0.05 μF	cer	25 V	110-019
C4	0.05 μF	cer	25 V	110-019
C5	0.05 μF	cer	25 V	110-019

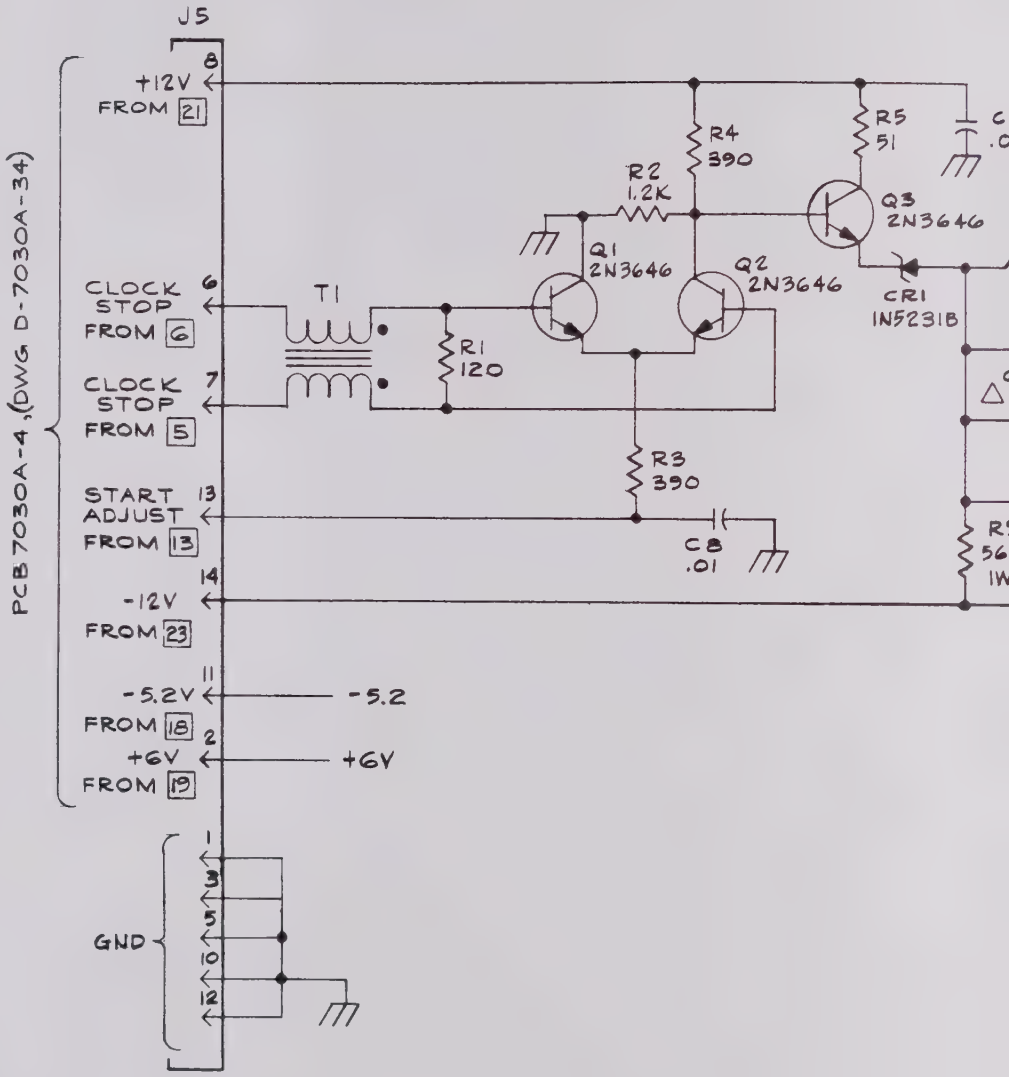
J5	Connector, 15-pin female	619-018

PANEL CONTROLS & CONNECTORS

DR-1	Oven Assembly	630-004
DS801	LED	416-002
J3	Ribbon Cable	626-008
J4	Ribbon Cable	626-023
J801	BNC Connector	624-002
J802	BNC Connector	624-002
J803	BNC Connector	624-002
J804	Pushbutton Switch SPDT	612-002
J805	Pushbutton Switch SPDT	612-002
J806	Pushbutton Switch SPDT	612-002
	Switch Cap	530-028
J901	Connector Female (36-pin)	619-001

R801	100 K	var	240-022
R802	100 K	var	240-022
R803	1 K	var	240-021

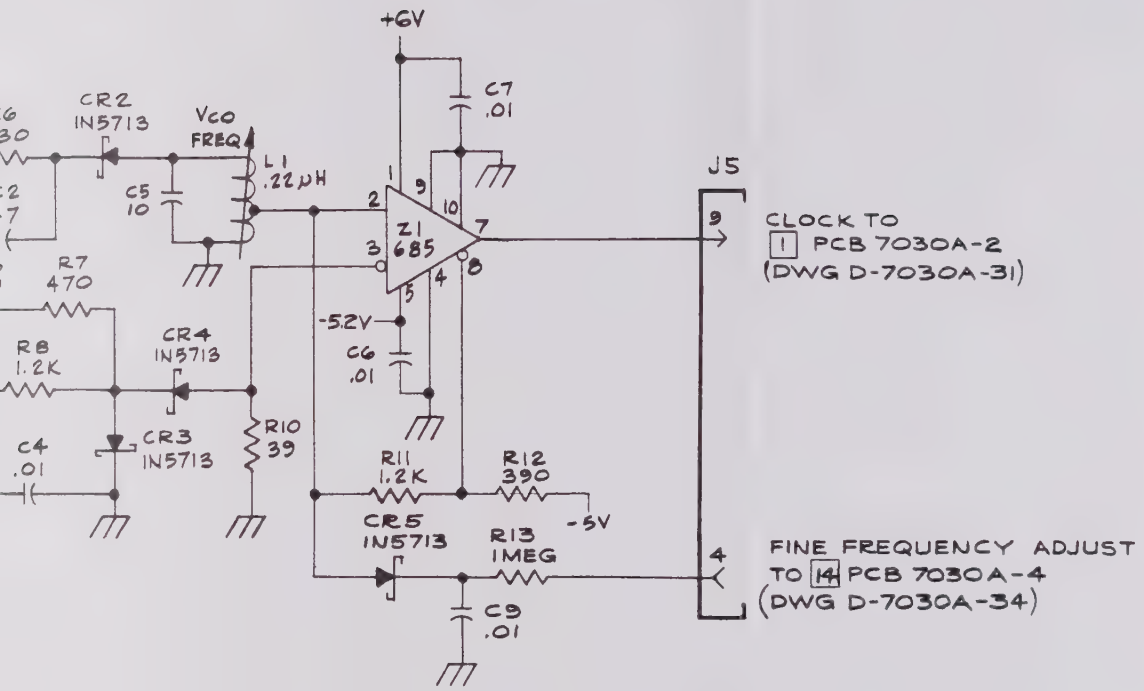
S801	Toggle Switch SPDT	611-001
S802	Toggle Switch SPDT	611-001
S803	Toggle Switch SPDT	611-001
S901	Switch, DPDT	613-003
T801-4	Core, Ferrite w/2 turns of wire, twisted pair	318-003
	Lens	516-001
	Knob, Initial Width	530-002
	Knob, Delay Width	530-002
	Knob, Tri. Level	530-002



NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTORS ARE 1/4 W, 5%
2. CAPACITORS <1.0 ARE IN μF, >1.0 ARE IN pF.
3. ☐ DENOTES PC BOARD TERMINALS.
4. △ DENOTES FACTORY SELECTED COMPONENT.

GRAPHICS, INC
R NO. 1856

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



REF. PCB 7030A-1

Z1	Z1	
T1	T1	
R1	R13	
Q1	Q3	
L1	L1	
J5	J5	
CR1	CR5	
C1	C9	
FIRST	LAST	OMITTED

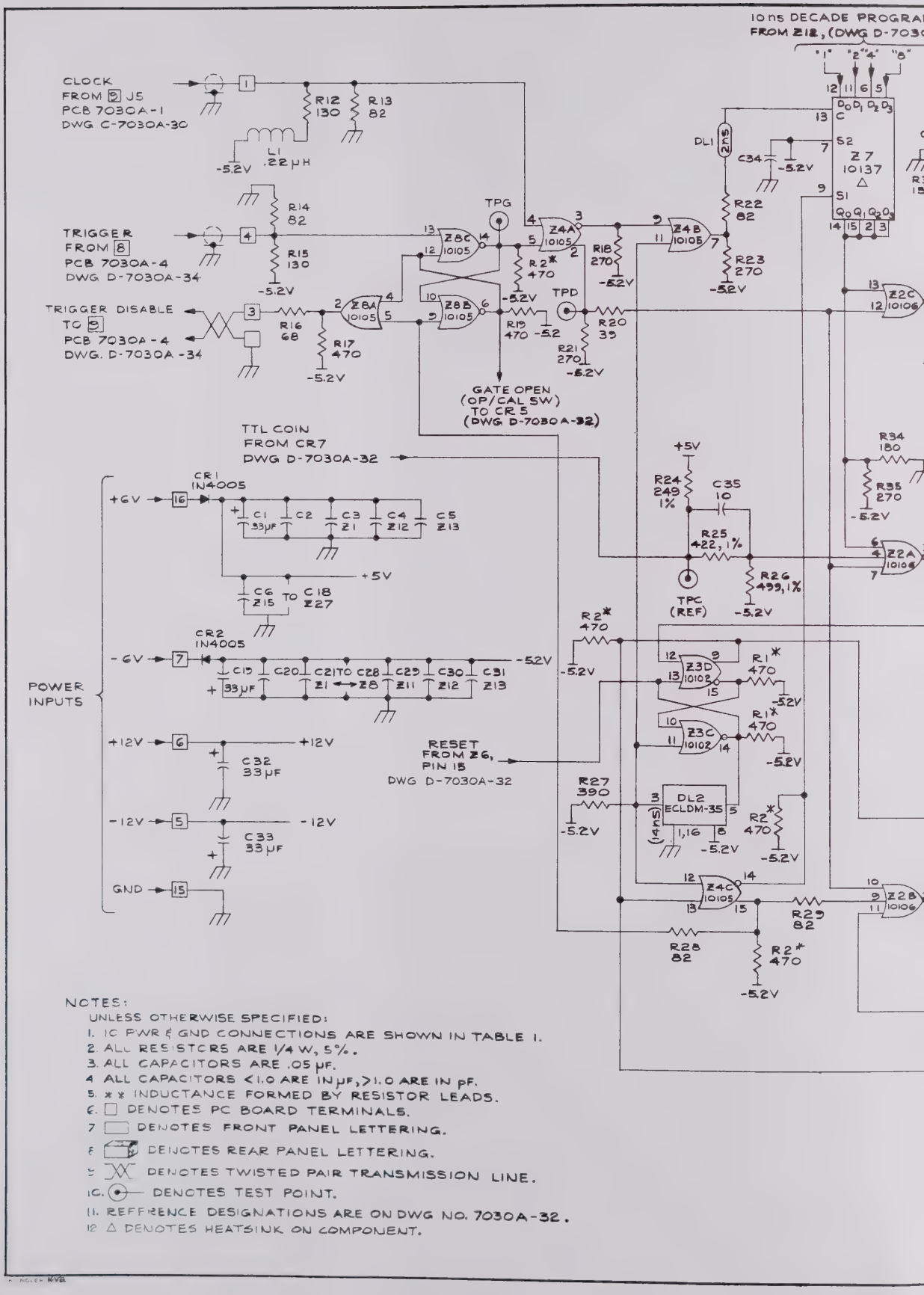
REFERENCE DESIGNATIONS

BNC **BERKELEY NUCLEONICS CORP.**
1198 TENTH ST., BERKELEY, CA 94710

SCALE NA	APPROVED BY EWK	DRAWN BY JWC
DATE 4-28-81		REVISED

DIGITAL DELAY GENERATOR MODEL 7030A

OSCILLATOR | C | DRAWING NUMBER 7030A-30


10 ns DECADE PROGRA
FROM Z12, (DWG D-703
CLOCK
FROM J5
PCB 7030A-1
DWG C-7030A-30
R12 130
R13 82
L1 .22 µH
-5.2V
TRIGGER
FROM 8
PCB 7030A-4
DWG D-7030A-34
R14 82
R15 130
TRIGGER DISABLE
TO 9
PCB 7030A-4
DWG. D-7030A-34
R16 68
R17 470
TPG
TPD
Z8C 10105
Z8A 10105
Z8B 10105
Z4A 10105
Z4B 10105
R18 270
R2* 470
R19 470
R20 39
R21 270
R22 82
R23 270
DL1 2ns
C34
Z7 10137
GATE OPEN
(OP/CAL SW)
TO CR5
(DWG D-7030A-32)
TTL COIN
FROM CR7
DWG D-7030A-32
CR1 IN4005
+6V
C1 33µF
C2
C3 Z1
C4 Z12
C5 Z13
C6 Z15 TO C18 Z27
CR2 IN4005
-6V
C19 C20 C21 TO C28 C29 C30 C31
33µF
Z1 Z8 Z11 Z12 Z13
POWER INPUTS
+12V
C32 33µF
-12V
C33 33µF
GND
+5V
R24 249 1%
C35 10
R25 422, 1%
R26 499, 1%
TPC (REF)
R34 180
R35 270
Z2A 10106
Z2C 10106
Z2B 10106
RESET
FROM Z6, PIN 15
DWG D-7030A-32
R27 390
DL2 ECLDM-35
(4ns)
Z3D 10102
Z3C 10102
Z4C 10105
R1* 470
R29 82
R28 82
NOTES:
UNLESS OTHERWISE SPECIFIED:
1. IC PWR & GND CONNECTIONS ARE SHOWN IN TABLE 1.
2. ALL RESISTORS ARE 1/4 W, 5%.
3. ALL CAPACITORS ARE .05 µF.
4 ALL CAPACITORS <1.0 ARE IN µF, >1.0 ARE IN pF.
5. * * INDUCTANCE FORMED BY RESISTOR LEADS.
6. □ DENOTES PC BOARD TERMINALS.
7 ▭ DENOTES FRONT PANEL LETTERING.
8 DENOTES REAR PANEL LETTERING.
9 DENOTES TWISTED PAIR TRANSMISSION LINE.
10. DENOTES TEST POINT.
11. REFFRENCE DESIGNATIONS ARE ON DWG NO. 7030A-32.
12 △ DENOTES HEATSINK ON COMPONENT.

BISHOP GRAPHICS, INC
REORDER NO. 1856

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ADDED HEATSINK TO Z7 PER ECO 85-009	5/22/85	JWL

A-32)

INS DECADE PROGRAM DATA
FROM Z13 (DWG D-7030A-32)

$\bar{D}_1$ D_1 D_{2A} $\bar{D}_{2A}$ D_4 $\bar{D}_4$ $\bar{D}_{2B}$ D_{2B}

-V_{BB1}

C37 56 CR3 IN5713
R31 86
C38 56
Z1B 10125
R32 2.7K
TPA (REF)
TTL CLOCK TO Z16, PIN 14 DWG D-7030A-32

R6* 180, 1%
R42 14K, 1%
R7 5K 2ns ADJ
R10 180, 1%
R50 14K, 1%
R9 5K 2ns ADJ
+12V
-12V
CW

R8 5K 4ns ADJ
R43 14K, 1%

Z10D
Z10A

C39 .001
C43 .001
C44 .001
C45 .001

Z9D 10815
Z9C 10515
Z11D 10515
Z11C 10515

H
DELAY LOGIC TO 32 PCB 7030A-4 (DWG D-7030A-34)

R33 14K, 1%
R5 5K INS ADJ

C40 .001
C46 .001
C47 .001
C48 .001

Z9A 10515
Z9B 10515
Z11A 10515
Z11B 10515

Z6A 10105
R36 2.7K
TPE
TPJ

R40 130
R44 130
R48 130
R53 130
**

DL3 1ns
DL4 2ns
DL5 4ns
DL6 2ns

R41 82
R45 82
R49 82
R54 82

-5.2V

R37 150
R38 56
CR4 IN5713
C41 82
Z1D 10125
TTL LOAD TO Z17, PIN 11 (DWG D-7030A-32)
TPB (REF)

C42 10
Z6B 10105
R39 1.5K
R3* 130
R3* 82
Z5D 10515
Z5C 10515
Z5A 10515
Z5B 10515
C49 10
C50
C51
INITIAL LOGIC TO 28 PCB 7030A-4 (DWG D7030A-33)

Z3B 10102
Z3A 10102
R1* 470
-6V

R55 178, 1%
Z10C LM348
V_{BB4} FROM Z5, PIN 9
R56 28K 1%
R4 5K (TO ADJ)

TABLE 1

IC POWER & GROUND CONNECTIONS					
IC REF. DESIG.	GND.	+5V	-5V	+12V	-12V
Z1, Z12, Z13	16	9	8		
Z2-Z5, Z11	1, 16		8		
Z10	—			4	11
Z14, Z22, Z27	7	14			
Z15-Z21, Z26	8	16			
Z23-Z25	10	20			

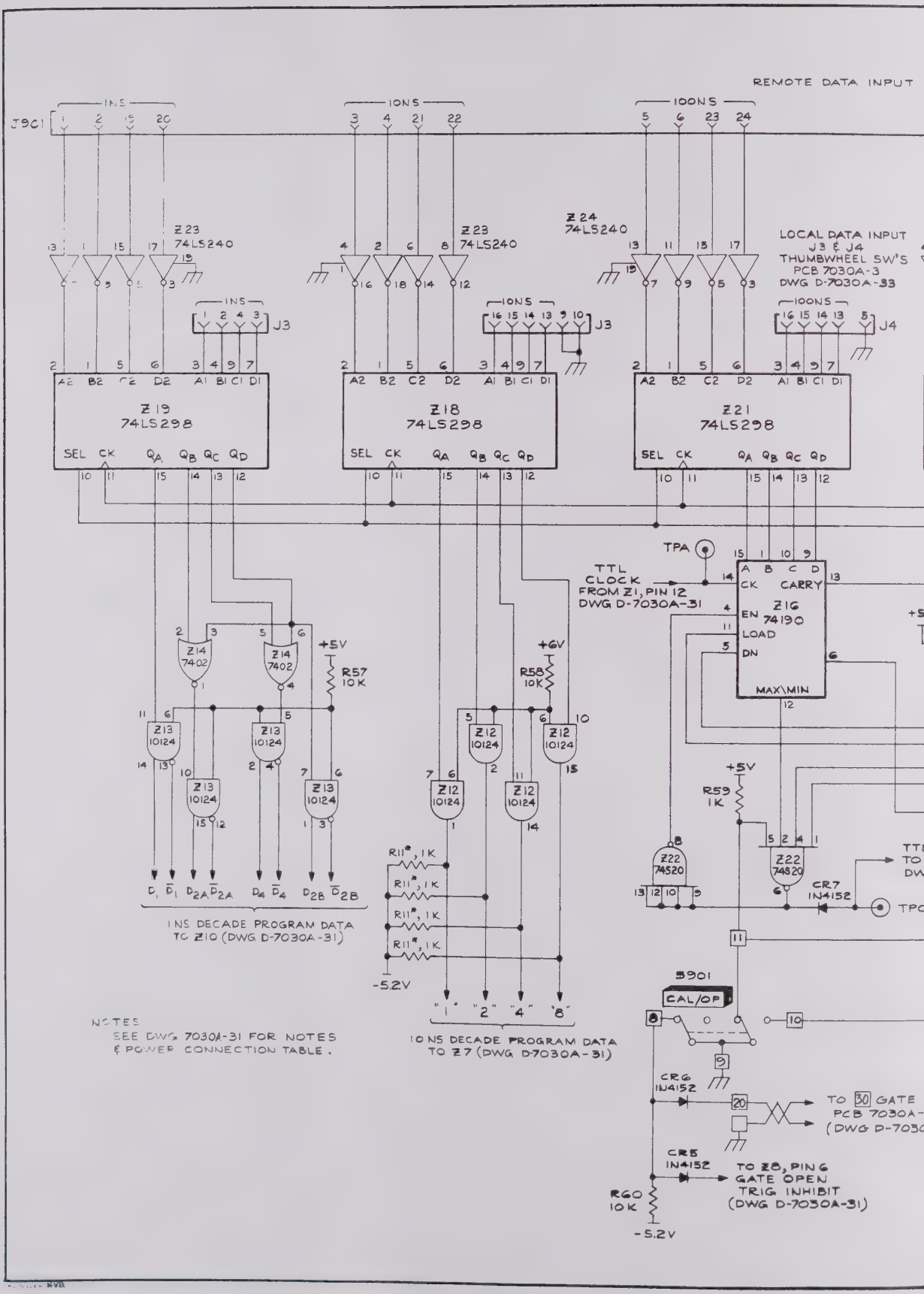
REF. PC BOARD 7030A-2

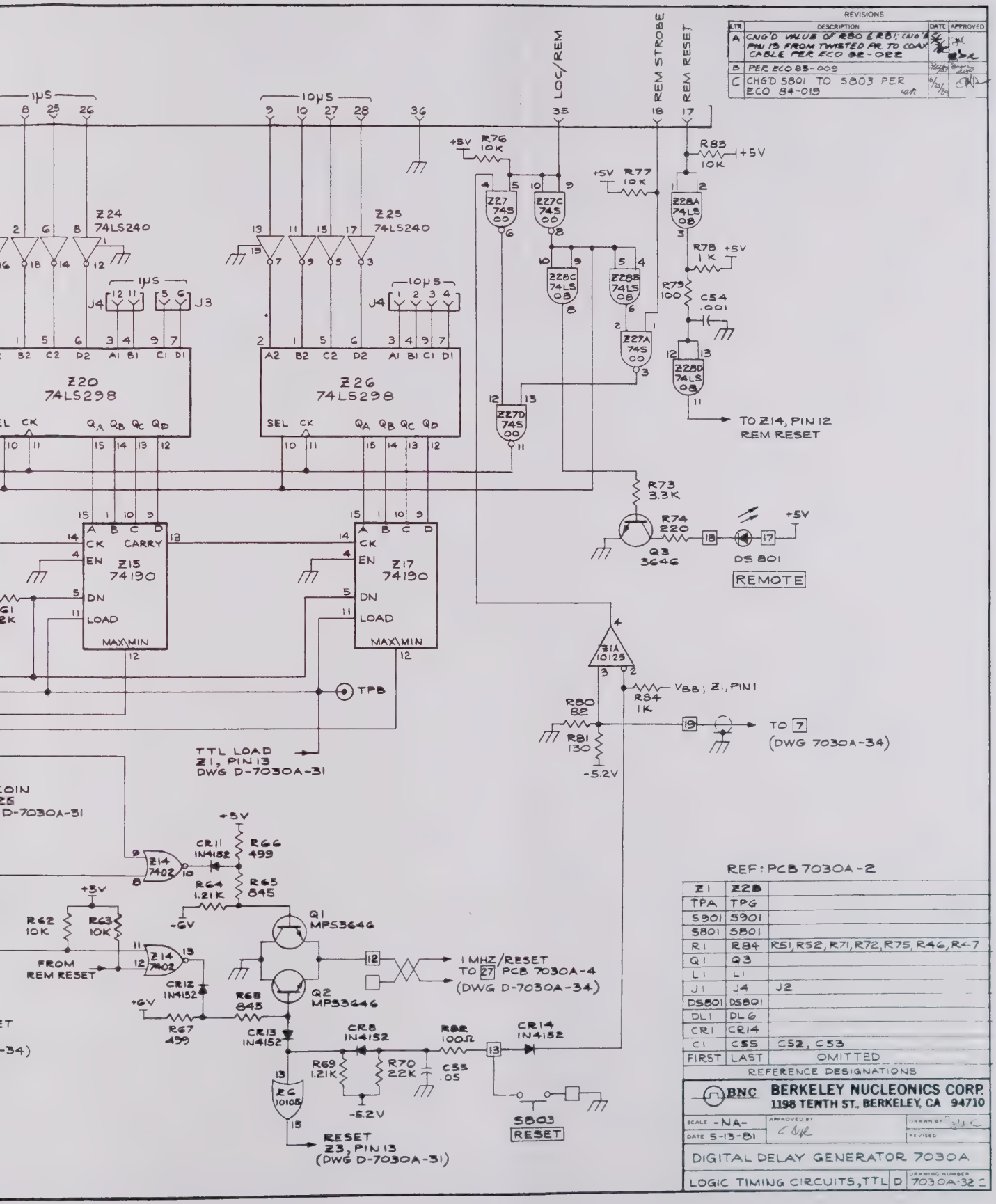
BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE -NA-	APPROVED BY	DRAWN BY JWL
DATE 4-13-81		REVISED

DIGITAL DELAY GENERATOR MODEL 7030A

LOGIC TIMING CIRCUITS, ECL | D | DRAWING NUMBER 7030A-31A


REMOTE DATA INPUT
J9C1
1NS
10NS
100NS
Z23 74LS240
Z24 74LS240
LOCAL DATA INPUT
J3 & J4
THUMBWHEEL SW'S
PCB 7030A-3
DWG D-7030A-33
J3
J4
Z19 74LS298
Z18 74LS298
Z21 74LS298
SEL CK QA QB QC QD
A1 B1 C1 D1
A2 B2 C2 D2
TPA
TTL CLOCK FROM Z1, PIN 12 DWG D-7030A-31
Z16 74190
A B C D
CK CARRY
EN
LOAD
DN
MAX\MIN
+5V
+6V
R57 10K
R58 10K
R59 1K
Z14 7402
Z13 10124
Z12 10124
Z22 74S20
CR7 1N4152
R11*, 1K
-5.2V
D1 D̄1 D2A D̄2A D4 D̄4 D2B D̄2B
1NS DECADE PROGRAM DATA TO Z10 (DWG D-7030A-31)
"1" "2" "4" "8"
10NS DECADE PROGRAM DATA TO Z7 (DWG D-7030A-31)
5901
CAL/OP
CR6 1N4152
TO 30 GATE PCB 7030A-
(DWG D-7030
CR5 1N4152
TO Z8, PIN 6 GATE OPEN TRIG INHIBIT (DWG D-7030A-31)
R60 10K
-5.2V
NOTES
SEE DWG 7030A-31 FOR NOTES & POWER CONNECTION TABLE.



REF: PCB 7030A-2

Z1	Z2B	
TPA	TPG	
S901	S901	
5801	5801	
R1	R84	R51, R52, R71, R72, R75, R46, R47
Q1	Q3	
L1	L1	
J1	J4	J2
DS801	DS801	
DL1	DL6	
CR1	CR14	
C1	C55	C52, C53
FIRST	LAST	OMITTED

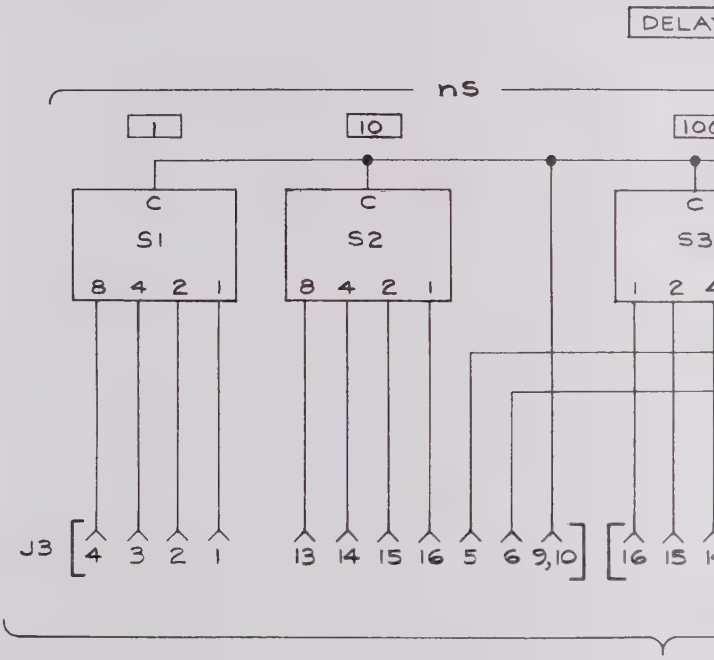
REFERENCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710

SCALE -NA- | APPROVED BY CWR | DRAWN BY | DATE 5-13-81 | REVISED

DIGITAL DELAY GENERATOR 7030A

LOGIC TIMING CIRCUITS, TTL | D | DRAWING NUMBER 7030A-32 C



NOTES:

1. [ ] DENOTES FRONT PANEL WORDING

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BISHOP GRAPHICS, INC
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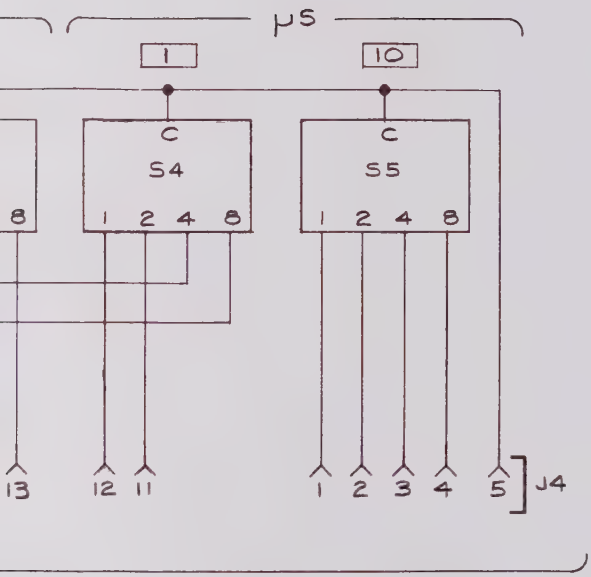
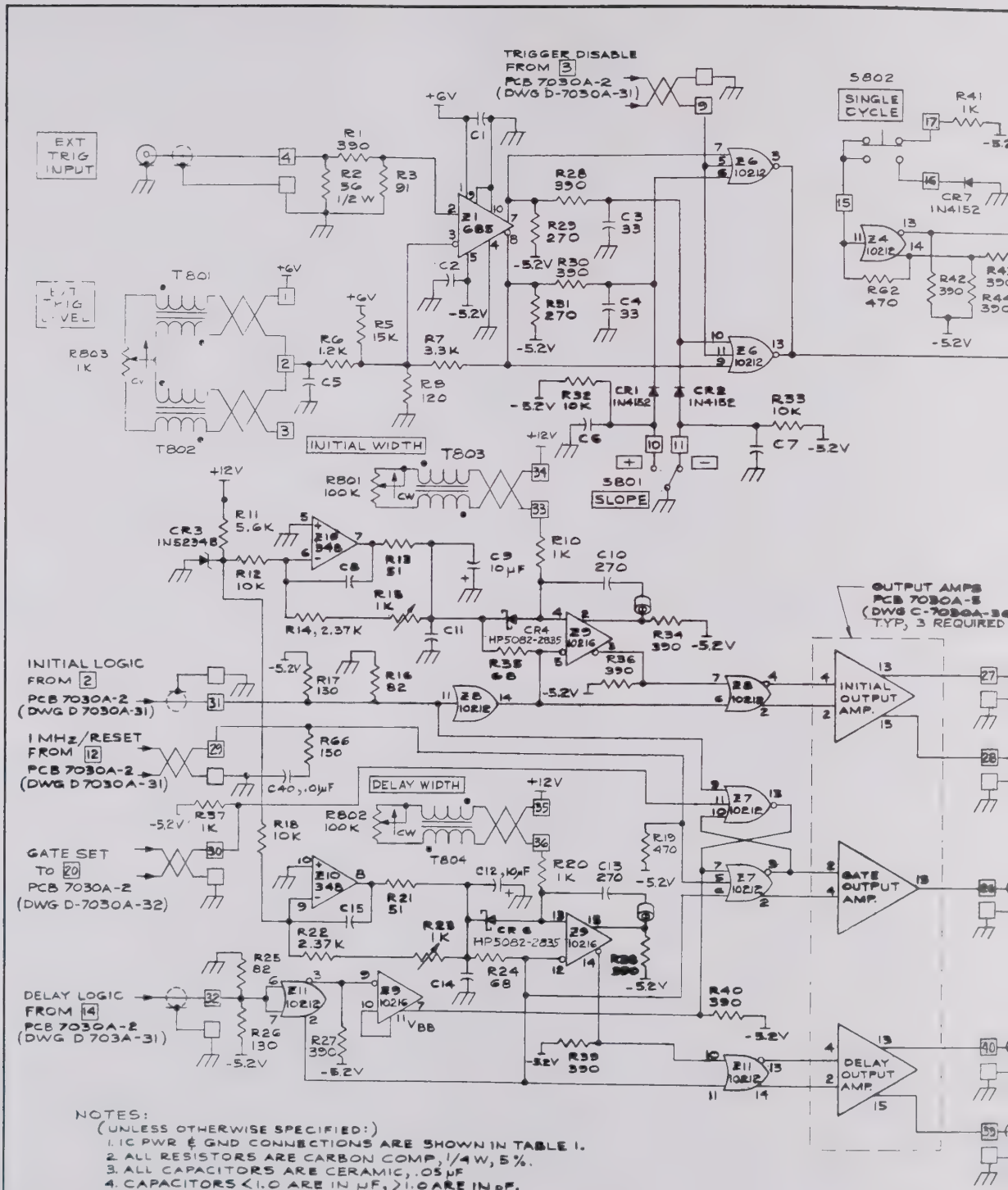
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



COUNTER & nS LINES
G D-7030A-32

REF. PCB 7030A-3

BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710		
SCALE: NA	APPROVED BY:	DRAWN BY
DATE: 4-28-81		REVISED
DIGITAL DELAY GENERATOR		MODEL 7030A
THUMBWHEEL SWITCHES	C	DRAWING NUMBER 7030A-33



NOTES:
(UNLESS OTHERWISE SPECIFIED:)

1. IC PWR & GND CONNECTIONS ARE SHOWN IN TABLE 1.
2. ALL RESISTORS ARE CARBON COMP, 1/4 W, 5%.
3. ALL CAPACITORS ARE CERAMIC, .05 μF
4. CAPACITORS < 1.0 ARE IN μF, > 1.0 ARE IN pF.
5. ☐ DENOTES PC BOARD TERMINALS.
6. ▭ DENOTES FRONT PANEL LETTERING.
7. ▱ DENOTES REAR PANEL LETTERING.
8. ⋈ DENOTES TWISTED PAIR TRANSMISSION LINE.
9. ⊕ DENOTES TEST POINT.
10. ⊖ DENOTES FERRITE BEAD.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PIN 7 CNG'D TO COAX w/FERRULS	5/12/82	
	B	PER ECO 82-030	3/29/83	
	C	ADDED "S802" TO "SINGLE CYCLE" SW. PER ECO 84-019	6.25.84 GR	
	D	ADDED R66 & C40 TO BD CONN 29	2/4/86 M	

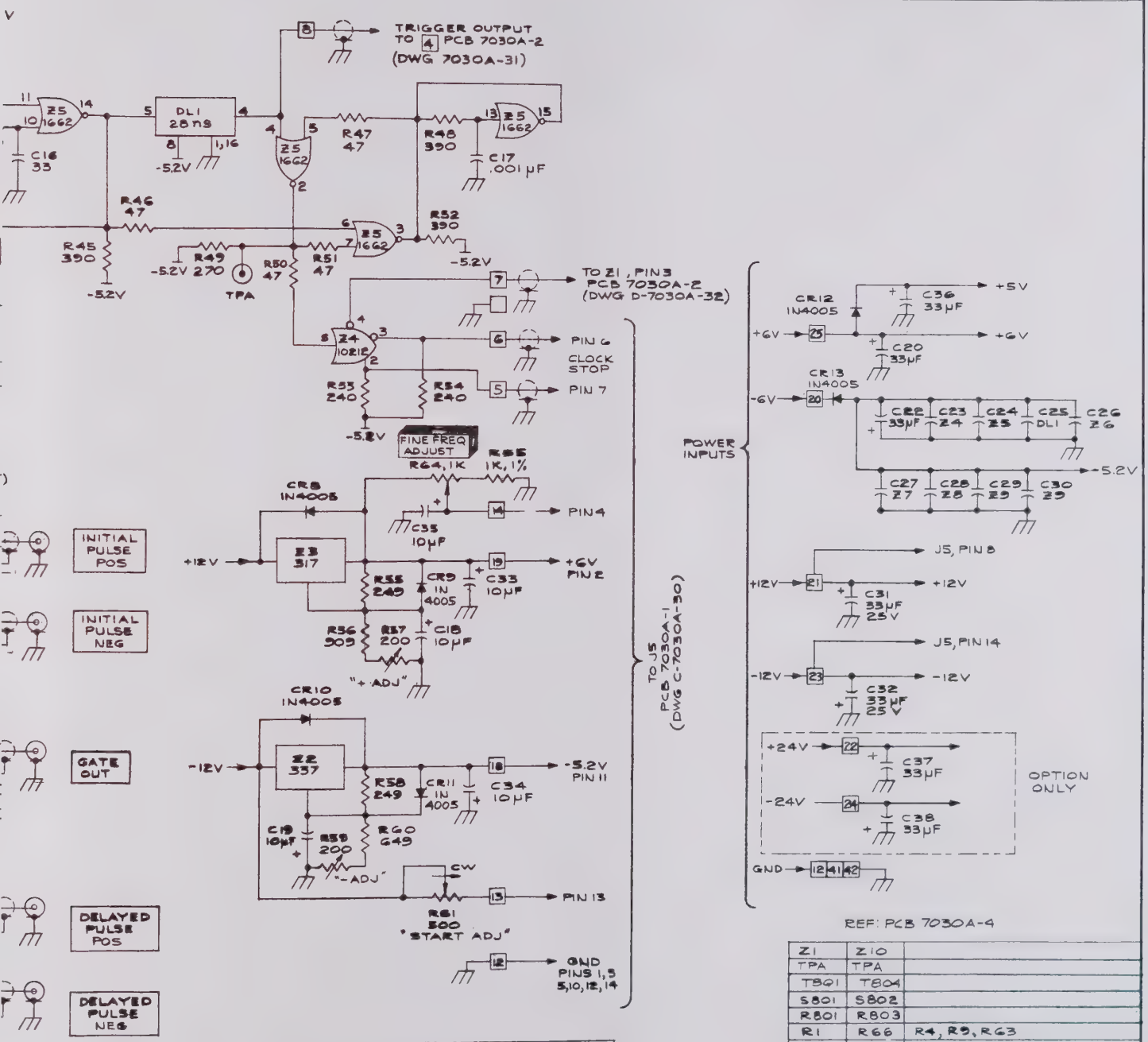


TABLE 1

IC POWER & GROUND CONNECTIONS

IC REF. DESIG.	GND	+5V	-5.2V	+6V	-6V	+12V	-12V
Z1	5,10		5	1			
Z4-Z9, Z11	1,16		8				
Z10		4					11
OUTPUT AMPS INITIAL, GATE, DELAY	3,7,9 12,14 16			5	1	6	10

REF: PCB 7030A-4

Z1	Z10	
TPA	TPA	
T801	T804	
S801	S802	
R801	R803	
R1	R66	R4, R9, R63
DL1	DL1	
CR1	CR13	CR5
C1	C40	C21, C39
FIRST	LAST	OMITTED

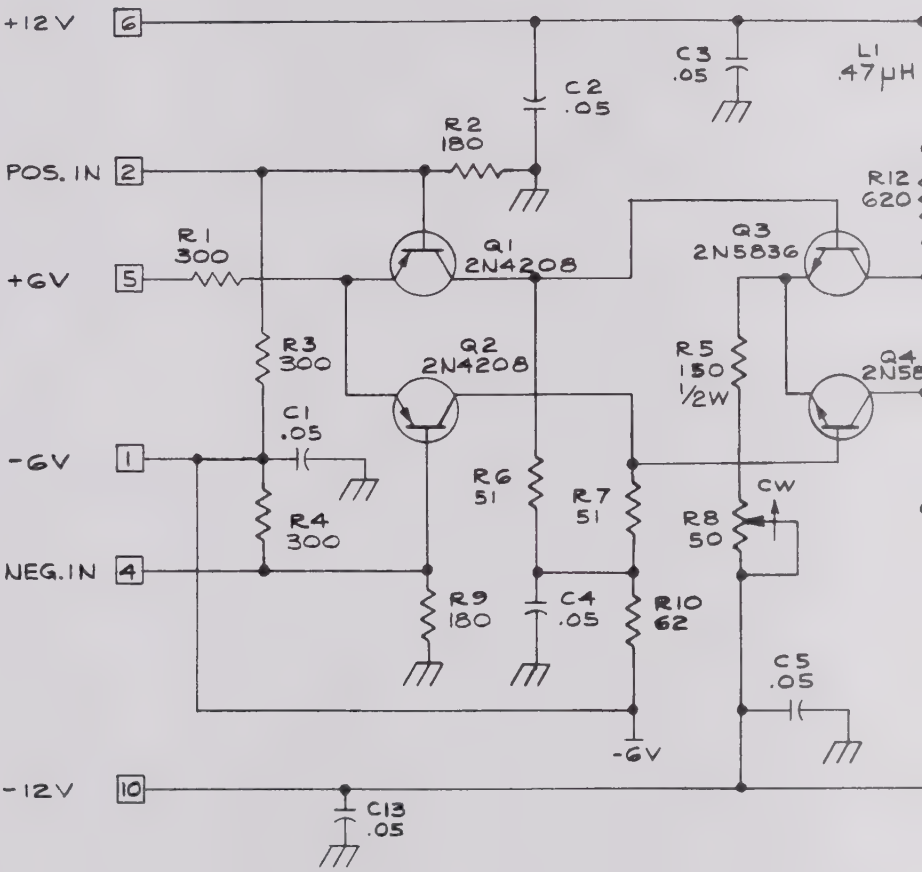
REFERENCE DESIGNATIONS

BNC BERKELEY NUCLEONICS CORP.
1198 TENTH ST., BERKELEY, CA 94710

SCALE -NA- | APPROVED BY | DRAWN BY | DATE | REVISED

DIGITAL DELAY GENERATOR 7030A

INPUT OUTPUT CIRCUITS | D | DRAWING NUMBER 7030A-34D



NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL RESISTORS ARE 1/4 W, 5%
2. RESISTOR VALUES ARE IN OHMS.
3. ALL CAPACITORS <1.0 ARE IN μF, >1.0 ARE IN pF

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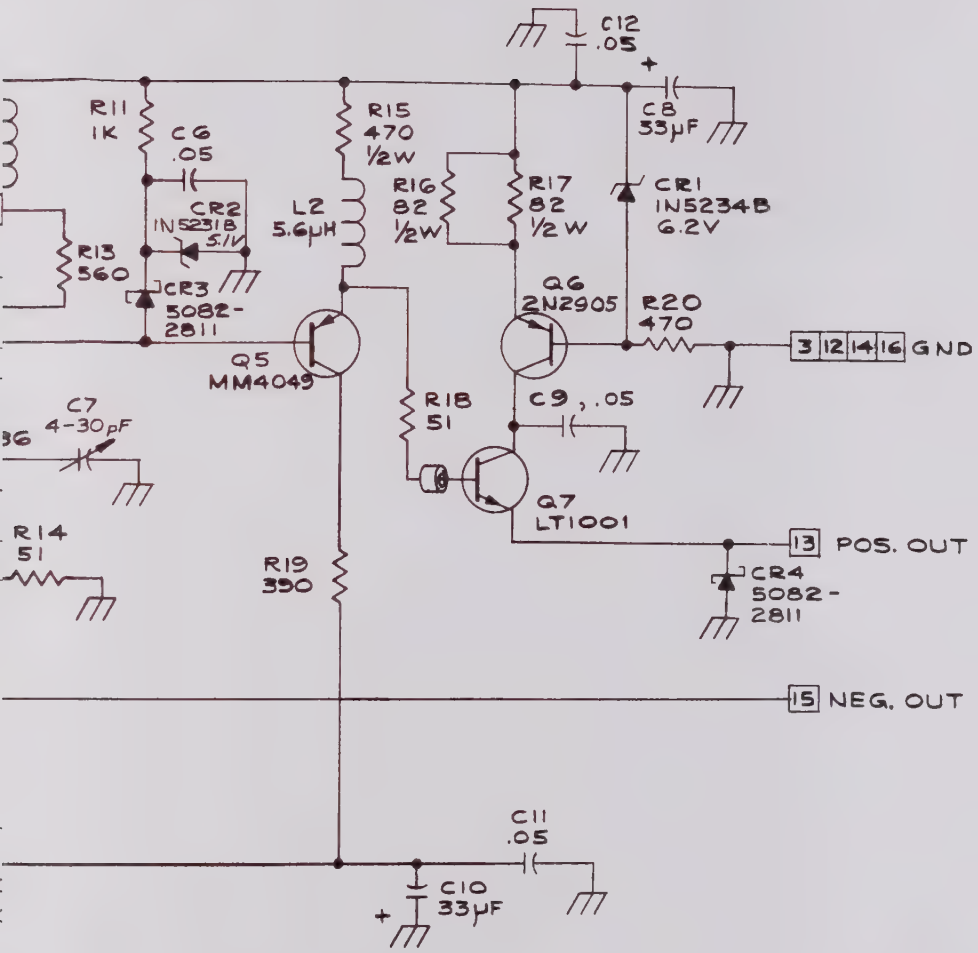
BISHOP GRAPHICS, INC
REORDER NO. 1856

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	CNG'D VALUES OF R2, 3, 4 & R9 PER ECO 82-023.	5/6/82	EDK
	B	CHG'D VALUE OF Q6 FROM 2N5583 TO 2N2905 PER ECO 84-002	1:19:84	[illegible]
	C	CHG'D C7 PER ECO 82-037	6-4-85	[illegible]



R1	R20	
Q1	Q7	
L1	L2	
CR1	CR4	
C1	C13	
FIRST	LAST	OMITTED

REFERENCE DESIGNATIONS

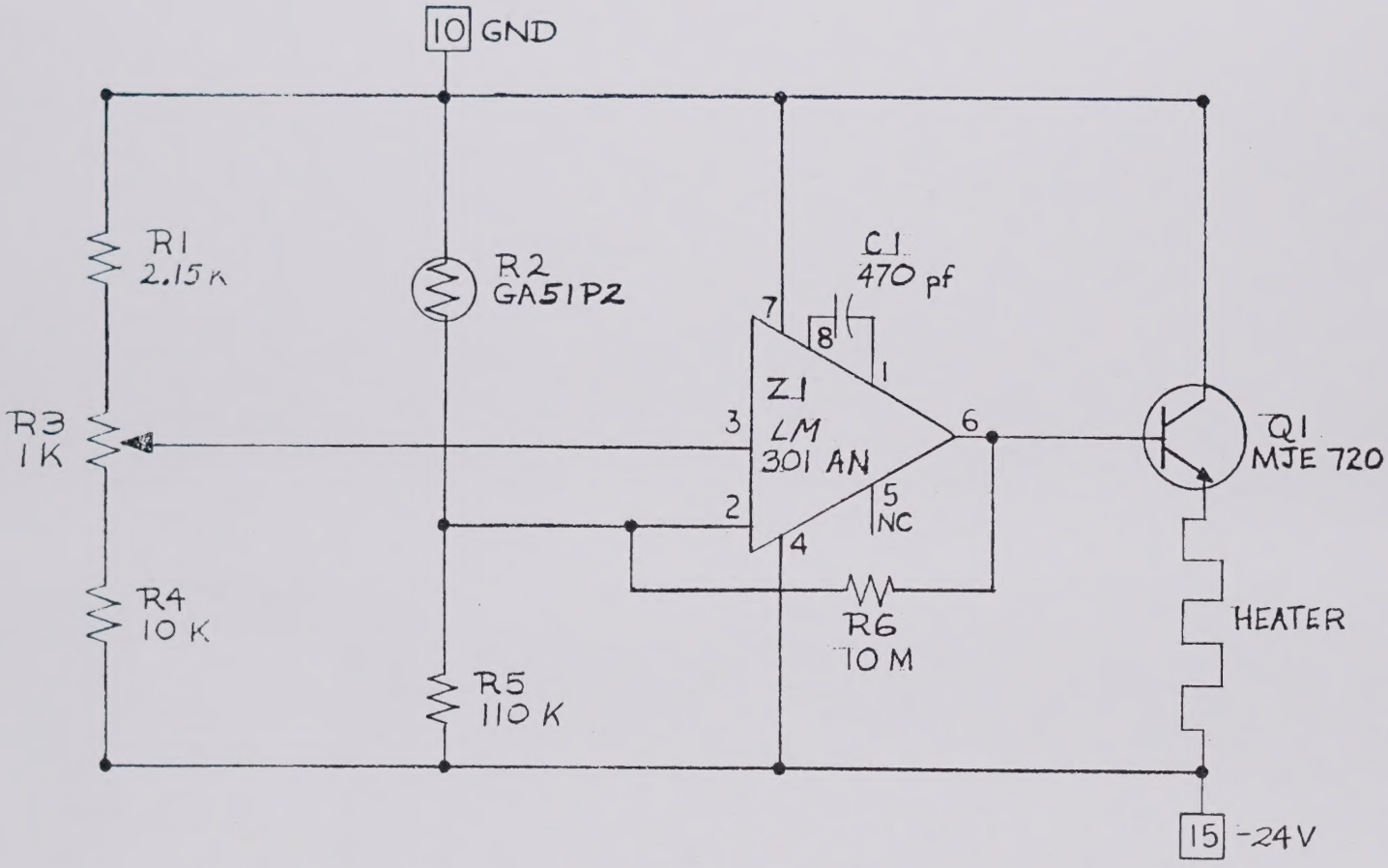
REF. PC BOARD 7030A-5

BNC **BERKELEY NUCLEONICS CORP.**
1198 TENTH ST., BERKELEY, CA 94710

SCALE: NA	APPROVED BY: EDK	DRAWN BY [illegible]
DATE: 9-8-81		REVISED

DIGITAL DELAY GENERATOR 7030A

OUTPUT AMPLIFIER | C | DRAWING NUMBER 7030A-36 C



BNC BERKELEY NUCLEONICS CORP. 1198 TENTH ST., BERKELEY, CA 94710		
SCALE: NONE	APPROVED BY:	DRAWN BY MJC
DATE: 3/15/73		REVISED
OVEN MODEL DR-1		
SCHEMATIC	A	DRAWING NUMBER DR1-15

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MP MASTER
MA32684